How to Build a Memristive Integrate-and-Fire Model for Spiking Neuronal Signal Generation

Sung Mo Kang, *Life Fellow, IEEE*, Donguk Choi, Jason K. Eshraghian, *Member, IEEE*, Peng Zhou, *Member, IEEE*, Jieun Kim, Bai-Sun Kong, *Member, IEEE*, Xiaojian Zhu, Ahmet Samil Demirkol, Alon Ascoli, *Member, IEEE*, Ronald Tetzlaff, *Senior Member, IEEE*, Wei D. Lu, *Fellow, IEEE*, and Leon O. Chua, *Life Fellow, IEEE*

***Abstract*— We present and experimentally validate two minimal compact memristive models for spiking neuronal signal generation using commercially available low-cost components. The first neuron model is called the Memristive Integrate-and-Fire (MIF) model, for neuronal signaling with two voltage levels: the spike-peak, and the rest-potential. The second model MIF2 is also presented, which promotes local adaptation by accounting for a third refractory voltage level during hyperpolarization. We show both compact models are minimal in terms of the number of circuit elements and integration area. Using the MIF and MIF2 models, we postulate the design of a memristive solid-state brain with an estimation of its surface area and power consumption. Analytical projections show that a memristive solid-state brain could be realized within (i) the surface area of the median human brain, 2,400cm^2, (ii) the same volume of the median human brain, and (iii) a total power budget of approximately 20 W using a 3.5 nm technology. Distinct from the past decade of memristive neuron literature, our benchmarks are attained using generic commercially available memristors that are reproducible using off-the-shelf components. We expect this work can promote more experimental demonstrations of memristive circuits that do not rely on prohibitively expensive fabrication processes.**

***Index Terms*— Neuromorphic computing, memristor, neuronal signal generation, minimal compact model, Hodgkin-Huxley model, physiological model, memristive solid-state brain.**

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Sung Mo Kang, Donguk Choi, and Peng Zhou are with the Department of Electrical and Computer Engineering, University of California at Santa Cruz, Santa Cruz, CA 95064 USA (e-mail: skang@ucsc.edu).

Jason K. Eshraghian is with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109 USA, and also with the Department of Computer Science and Software Engineering, The University of Western Australia, Perth, WA 6009, Australia (e-mail: jeshraghian@gmail.com).

Jieun Kim and Bai-Sun Kong are with the Department of Electrical and Computer Engineering, Sungkyunkwan University, Suwon 16419, South Korea (e-mail: bskong@skku.edu).

Xiaojian Zhu is with the Chinese Academy of Sciences, Ningbo 315201, China.

Ahmet Samil Demirkol, Alon Ascoli, and Ronald Tetzlaff are with the Chua Memristor Center, Technical University of Dresden, 01069 Dresden, Germany.

Wei D. Lu is with the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, MI 48109 USA.

Leon O. Chua is with the Department of Electrical Engineering and Computer Science, UC, Berkeley, CA 94720 USA.

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I. Introduction

NEUROMORPHIC computing is pursued to overcome the limitations of von Neumann architecture and Moore's law [1], [2]. Harnessing brain-inspired properties such as in-memory computing, spike-based encoding, and adaptation has bolstered energy-delay efficiency by orders of magnitude for certain classes of computation [3], [4]. Architectural emulation of the brain is naturally complemented by device-level optimization. The use of functional blocks in integrated circuits that behave similarly to the core units of the central nervous system (neurons and synapses) may enable circuits to efficiently accomplish tasks associated with human cognition [5], [6].

The memristor was first introduced by Chua [9] as a circuit element as fundamental as *R*, *L*, and *C*, the notion of which was generalized by Chua and Kang in 1976 [10].The demonstration of nanoscale memristors fabricated by Strukov, *et al.* [11] propelled a myriad of research and applications in memristive storage-class memory, sensing, logic operations and memcomputing [12]–[18]. In more recent times, memristors have become available through commercial fabrication processes [19], [20] and are commonly used in non-volatile resistive switching arrays as resistive random-access memory (RRAM) [21], [22].

Memristor technologies have ushered in new approaches for emulating both biological neurons and synapses [23]–[26]. Synaptic plasticity has been demonstrated in memristors by using spike trains to potentiate or depress conductance [27]. Potentiation and depression have been observed in synaptic memristors between pre-synaptic and post-synaptic neurons [28]. A variety of approaches are used to design electronic neurons that generate spiking signals and to implement synaptic interconnects, with the emphasis of using memristors on low energy consumption and high packing density.

There is a high barrier to accessing experimental data and hardware for prototyping memristive circuits. Most experimental demonstrations rely on specialized fabrication processes. The reproducibility challenge is compounded by limited accessibility to commercial, low-cost, and robust

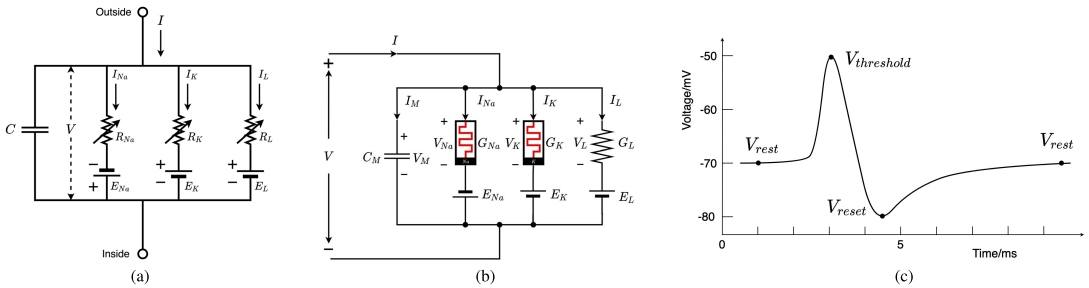

Fig. 1. Hodgkin-Huxley neuron model [7]. (a) An equivalent circuit for the HH model [7]. (b) An equivalent circuit for the memristive HH model [8]. (c) An action potential waveform showing rest, threshold and reset potentials.

discretely packaged memristors [29], [30]. The challenge in developing hardware prototypes has made experimental validation difficult.

Beyond neural network acceleration, the design of a solid-state brain that can harness the neural code in an unsupervised manner has received increasing attention as a way to handle huge sensory input data without being thwarted by the von Neumann bottleneck [31]. The solid-state brain mimics the structure of the cerebral cortex by connecting neurons with a large fan-out of plastic synapses. It is conjectured the neurons and synapses can be realized with memristors integrated with a CMOS process. However, the design of a large-scale solid-state brain remains elusive in neuromorphic computing due to the enormous overheads associated with mimicking the surface area of neural tissue, constrained power consumption, routing and massive parallelism of synaptic connections.

In this paper, we aim to overcome several of these barriers by introducing the memristive integrate-and-fire (MIF) neuron circuit model. Firstly, we experimentally demonstrate the generation of spiking neuronal signals using our MIF and MIF2 models implemented with commercially available, low-cost components. The vast literature on memristive neuron circuits and neuristors are typically limited by either being simulation-only idealized studies, or rely on device-dependent characteristics not readily accessible to the broader research community. With similar neuron circuits presented in the past, we demonstrate the operation of the MIF and MIF2 circuits without specialized fabrication processes that make our results reproducible by an amateur in hardware prototyping on a tight budget. We develop a circuit-theoretic foundation of our models that mimic the passive membrane model [32], and by extension, our model demonstrates minimal complexity and integration area. An experimental energy analysis is conducted, showing that a scaled-up system with the same order of neurons as in the human brain consumes approximately an equivalent amount of power. We present our results with the hope that it fosters more experimental demonstrations of bio-inspired memristive circuits and systems in the future.

This paper is organized as follows: section II outlines conventional neuronal circuit models, providing a background of the Hodgkin-Huxley (HH) and Leaky Integrate-and-Fire (LIF) models. Section III presents the MIF and MIF2 models, with a comprehensive characterization of their operating modes and their minimality. Each model circuit is analyzed as a simplified linear circuit for both on and off states of memristors before conducting a more precise nonlinear analysis with CAD tools. A scaled implementation demonstrating the feasibility of meeting the requirements for a VLSI implementation of a memristive solid-state brain is provided in section IV, followed by conclusions in section V.

II. Background

A. The Hodgkin-Huxley Neuron Model

The physiologically derived HH model [7] is among the most pervasive neuron models used to simulate spiking neuronal signals, or action potentials. Fig. 1(a) shows its equivalent circuit. The sodium and potassium channels, depicted by conductors G_{Na} and G_{K}, were described by Hodgkin and Huxley as time-varying nonlinear conductors.

Noble reduced the HH model by setting the leakage channel conductance to $G_{\mathrm{L}} = 0$. The reduced HH model provides the best fit for human cardiac action potentials [33]. Chua and Kang identified G_{Na} and G_{K} as memristors [10], and presented a comprehensive circuit-theoretic foundation for the HH axon circuit model, shown in Fig. 1(b). It should be noted that this analysis was focused on the memristive properties of the sodium and potassium conductive channels used in the HH model, without modifying the conductors' model equations.

The membrane voltage $V(t)$ from the HH equations is known to accurately replicate the physiological action potential. The HH system is a highly stiff system of ordinary differential equations, and there is no closed-form solution. For a more tractable analysis, many modifications of the model have been proposed. Fig. 1(c) illustrates a typical approximation of the action potential. It shows a rest-potential V_{rest}, a reset-potential V_{reset} below the rest-potential, which follows in time after the membrane reaches a threshold-potential $V_{\mathrm{threshold}}$.

B. The Leaky Integrate-and-Fire (LIF) Model

Where simpler models are desired that do not consider individual ion channels, the LIF model shown in Fig. 2(a) has been broadly adopted as a simple neuron model [32], [36]. It is straightforward to integrate LIF neurons into modern deep learning frameworks [37], while the HH model is better tailored for accurate physiological emulation. Input synaptic current $I(t)$ can be described by using a time-varying alpha function in (1), although a saw tooth or a pulse function can be used as an alternative. The plot of (1) is shown in Fig 2(b).

$$I(t) = I_0 \cdot \mathrm{e} \cdot (t/\tau_\alpha) \cdot e^{-\frac{t}{\tau_\alpha}} \text{ for } t > 0 \tag{1}$$

Note the first, non-italicized 'e' is the Neper constant. Under the influence of $I(t)$, $V(t)$ across the capacitor C is charged up with an RC time constant. When $V(t)$ reaches a threshold-potential$V_{\mathrm{threshold}}$, the charge accumulated on C must discharge until a rest-potential V_{rest} is reached. Figs. 2(c-d) illustrate this operation for the case of a DC input current and a zero rest-potential ($E_{\mathrm{rest}} = 0$) [34]. However, if $I(t)$ does not charge C to the level $Q_{\mathrm{peak}} = V_{\mathrm{threshold}}C$ with $V_{\mathrm{threshold}}$ representing a voltage level corresponding to V_{th} in

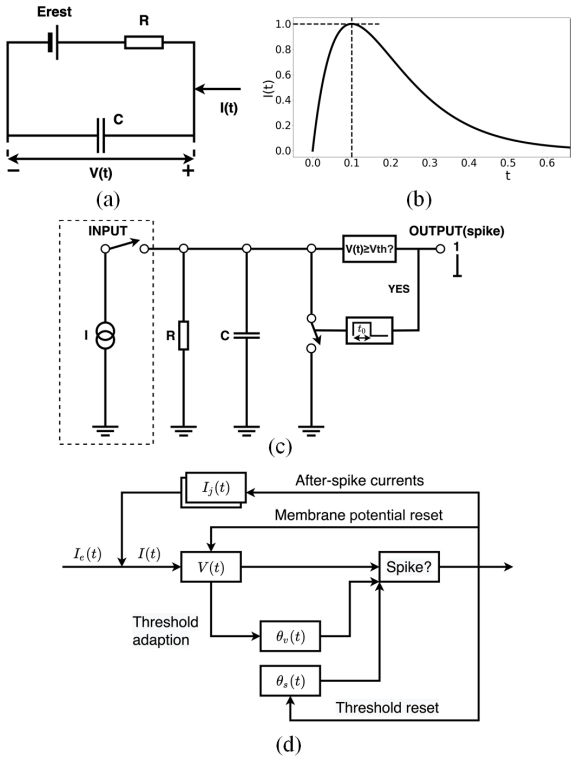

Fig. 2. The leaky integrate-and-fire (LIF) neuron model. (a) Schematic of the LIF electrical model. (b) Input current in the form of an alpha function ($\tau_{\text{alpha}} = 0.1$, $I_0 = 1$) (c) Controlled spiking in the LIF model with a comparison of membrane potential and threshold at each time step. When a spike is triggered, a voltage-controlled switch discharges C for the duration of the refractory period t_0. Reproduced with permission from Tal and Schwartz, [34]. (d) A generalized LIF model with threshold control. Figure from Teeter *et al.* (2018) reproduced under a CC BY 4.0 license [35].

Fig. 2(c), the capacitor would fail to discharge to reproduce the biological reset condition. In Fig. 2(c), the inequality $V(t) \geq V_{\text{threshold}}$ must be evaluated using an active circuit such as a comparator. Each time the threshold is reached, the membrane potential is reset. Thus, the generalized LIF model requires additional overhead, as depicted in Fig. 2(d). In the generalized LIF model, the membrane potential can be pulled down below the rest-potential using adaptive control, external to the LIF model. This external control requires sophisticated, active circuits composed of MOS transistors, resistors, and even a silicon-controlled rectifier (SCR).

C. Memristors

The memristor was initially postulated as a fundamental circuit component that relates flux to charge [9]. This linkage would allow a driving voltage (or current) to program the resistance, which would then remain constant in absence of any additional modulation. The flux-charge linkage was generalized in [10] to encompass alternative mechanisms of resistive switching. An electric field can be used to modulate the resistance of a memristor through a variety of physical means, including ionic transport [11], formation of conductive filaments [38], joule-heating (inducing phase change) [39], and spin-transfer torque [40]. A memristor is now broadly classed as a non-volatile electronically-variable resistive memory. Analogously, the conductance of a synaptic channel between a pair of neurons is modulated by action potentials, which is a voltage spike that results in the build-up of an electric field and has led to the broad adoption of memristive synapses that retain memory of their synaptic strength.

Resistance switching may be incremental/soft (analog) or hard (digital). Analog switching may take place across a broad spectrum of conductance states that allows gradual modulation of conductance, in a manner that resembles synaptic weight updates [41]–[43]. Hard switching between two resistance states are applicable in neuronal spike generation mechanisms, where the absence of an action potential corresponds to a resting state, and the generation of an action potential arises once the memristor has been switched [44]. Memristors generally include devices that exhibit transient memory effects across a variety of time scales [27], [45], [46], which can be likened to transient behaviors in neurons, such as spike-frequency adaptation, homeostatic thresholds, and dendritic pruning.

Recently, an integrated system using volatile memristor$-C$ LIF neurons and memristor synapses was shown to mimic particular cortical functions [35]. It generated spiking signals with two voltage levels (the threshold potential and the rest potential) by applying careful timing control on the input signal, and mimics hyperpolarization to the reset-potential shown in Fig. 1(c) by using post-synaptic currents. Here, the memristor must be volatile and is thus material-dependent to instil a relaxation time. To remove such limitations as in our contribution, we introduce the MIF model shown in Fig. 3(a), which allows a broader class of memristors to be integrated as neurons. We demonstrate our results on low-cost and commercially available memristors, and seek to eliminate the stigma that memristive research is either performed using idealized simulations or requires expensive fabrication facilities.

III. The Memristive Integrate-and-Fire Neuron Model

In this section, we present two versions of the memristive neuron model. Both exhibit threshold firing and a reset mechanism that is required by integrate-and-fire neurons; the subtle difference is that the second version adds a sub-rest potential after spiking to the first version. This can be thought of as a refractory action induced by an additional memristor and a DC voltage source. In practice, such use of a DC source will not require a separate battery for each neuron. Rather, a DC voltage supply rail would be used, which will add some overhead for physical connections, but is much simpler and less area consuming than placing separate DC batteries. We first analyze the MIF and MIF2 circuits using simplified on-off state-dependent linear circuits. Following that, a precise nonlinear analysis in Cadence/Spectre is undertaken.

A. MIF Neuristor

In place of the resistor R in the LIF model shown in Fig. 2(a), the first version of the MIF model in Fig. 3(a) uses a single memristor. This model does not require external adaptive control, to discharge the capacitor when the action potential reaches $V_{\text{threshold}}$. The MIF model is device-agnostic; as long as the energy supplied is sufficient for bipolar resistance switching, the circuit will be capable of action potential generation. This is a significant improvement in view of the integration complexity and packing density, since the implementation of an adaptive control circuitry requires the CMOS substrate to be connected through via holes to higher layer memristors. Prior implementations of similar neuristor circuits are typically dependent upon restrictive volatile characteristics, with relaxation times far smaller than any RC delay present in the neuron [47], [48]. The MIF neuron model generalizes

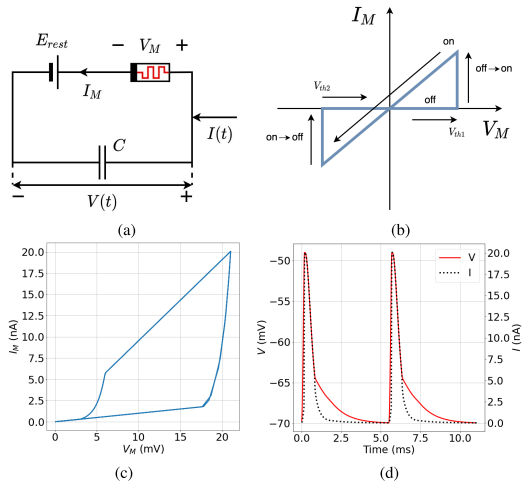

Fig. 3. The memristive integrate-and-fire (MIF) neuron model. (a) The MIF model replaces the R of the LIF model with one memristor. (b) $I-V$ curve of a simple digital memristor. (c) The measured $I-V$ curve of the volatile memristor selector that is used to obtain the MIF simulation results in (d). In Fig. 3(d), $I(t)$ is the current described by (1).

previous volatile memristor-based designs to reproduce the dynamics of biological neurons more closely, and the following work fosters reproducibility by using commercially available components.

Practical considerations on cycle-to-cycle variations and the ratio of pre- and post- switching resistances will serve to alter the spike shape. For a MIF circuit with a volatile memristor, a DC E_{rest}-source is sufficient to generate spikes under a sufficient input current. For instance, under DC current input of an appropriate magnitude, the MIF circuit, particularly with locally active memristors [49], can generate oscillatory spiking signals. If a non-volatile memristor with a negative reset-voltage is present in the MIF circuit, then a suitable voltage pulse must be added to the DC E_{rest}-battery to reset the memristor back to its initial off-state after emitting a spike. We experimentally demonstrate this need in section IV. When the membrane potential attains the value $V_{\text{threshold}}$, the memristor sets and turns onto its low-resistance state, providing the capacitor with a low-resistance pathway for discharging. However, the resulting progressive decrease of the membrane voltage $V(t)$ toward a rest level V_{rest} is insufficient to switch the non-volatile memristor back to its original off-state condition, unlike for a volatile memristor. In absence of volatility, a voltage pulse needs to be added to the DC level E_{rest} to reset the non-volatile memristor, but still no additional control circuitry is needed on a per-neuron basis. If a memristor with an S-shaped locally active DC $I-V$ characteristic is used, then both off-to-on and on-to-off resistance switching phenomena occur under a positive voltage stimulus, i.e., both the set and reset voltages of this device feature a positive polarity. We can formulate a state equation for the MIF model in Fig. 3(a) in terms of the voltage $V(t)$ across the capacitor C (equivalently, the membrane potential), the memristor resistance (memristance) R_{M}, the voltage source E_{rest}, and the input current $I(t)$:

$$C\frac{V(t)}{dt} = -\frac{V(t)-E_{\text{rest}}}{R_{\text{M}}(x, V(t))} + I(t) \tag{2}$$

Here, $R_{\text{M}}(x,\ V(t))$ is a voltage-controlled memristance, where x represents the internal state of the device. Equation (3) describes a digital memristive switch (see Fig. 3(b) for an example of a simple $I-V$ characteristic chosen for simple analysis). Note that, due to the difference between the device set and reset thresholds, we denote the memristor set voltage as V_{th1}, and the memristor reset voltage as V_{th2} in Fig. 3(b). Furthermore, V_M is the potential across the memristor and $V_{\text{threshold}}$ is the membrane threshold voltage, which is distinct from both the memristor set and reset thresholds. The voltage across the memristor is the difference between the membrane potential and DC potential $V_M = V(t) - E_{\text{rest}}$. As such, we can state that for the memristor with a simple resistance-switching $I-V$ characteristic shown in Fig. 3(b),

$$\begin{aligned} R_M &= R_{\text{off}} \text{ for } V_{\text{th2}} < V_M < V_{\text{th1}} \text{ as } V_M \text{ increases,} \\ R_M &= R_{\text{on}} \text{ for } V_{\text{th2}} < V_M < V_{\text{th1}} \text{ as } V_M \text{ decreases.} \end{aligned} \tag{3}$$

It should be noted that the constraints in (3) can be stated in terms of $V(t)$ since $V(t) = E_{\text{rest}} + V_M$.

Assuming an initial membrane potential $V(0) = V_{\text{rest}}$, $V(t)$ may increase due to an incoming current spike. Accordingly, V_M will increase as long as the memristor state does not switch. Therefore, while $V_{\text{rest}} \le V(t) \le V_{\text{threshold}}$, for the case of Fig. 3(b), (2) can be recast as

$$C\frac{V(t)}{dt} = -\frac{V(t)-E_{\text{rest}}}{R_{\text{off}}} + I(t). \tag{4}$$

For simplicity, it is reasonable to approximate the incoming current function by $I(t) = I_o[\text{sign}(t) - \text{sign}(t - T_W)]/2$, a rectangular pulse of width T_W. For $0 \le t \le T_W$, (4) becomes

$$C\frac{V(t)}{dt} = -\frac{V(t)-E_{\text{rest}}}{R_{\text{off}}} + I_0. \tag{5}$$

The solution of (5) for $0 \le t \le T_W$ is

$$V(t) = V_{\text{rest}}e^{-\frac{t}{\tau}} + (E_{\text{rest}} + R_{\text{off}}I_0)(1 - e^{-\frac{t}{\tau}}) \tag{6}$$

where $\tau = R_{\text{off}}C$. This equation holds true while the memristor remains in the off state: $V_M < V_{\text{th1}}$. We can find the time t_{clamp} required for $V(t)$ to reach $V_{\text{threshold}}$ by using (6):

$$t_{\text{clamp}} = R_{\text{off}}C\ln\left[\frac{R_{\text{off}}I_0 - (V_{\text{rest}} - E_{\text{rest}})}{R_{\text{off}}I_0 - (V_{\text{threshold}} - E_{\text{rest}})}\right] \tag{7}$$

For $T_W > t_{\text{clamp}}$, $V(t)$ can increase beyond $V_{\text{threshold}}$ without resistance-switching. Thus, in the MIF model, the memristor connected to E_{rest} must switch to R_{on} at $V(t) = V_{\text{threshold}}$ so that $V(t)$ can decrease towards V_{rest}, which should counteract the influence of any non-zero input current tail. Equation (2) is valid in the case where the memristor features linear $I-V$ characteristics for both on and off states. For nonlinear analog memristors, we use computer simulation for accurate circuit analysis. We used the Cadence/Spectre simulator for a detailed analysis of the MIF circuit with a volatile memristor selector featuring the nonlinear $I-V$ characteristic shown in Fig. 3(c) [50].

Figure 3(d) shows that as the capacitor voltage $V(t)$ rises and reaches $V_{\text{threshold}}$, the voltage across the memristor V_M reaches the set-voltage V_{th1}. When the memristor enters the set-state, R_M switches from R_{off} to R_{on}. Following this change, the voltage across the capacitor starts to fall toward V_{rest}, initially with time constant $R_{\text{on}}C$, and later $R_{\text{off}}C$ since V_{th2} is non-negative and small in the volatile selector device. In other words, as the voltage across the memristor V_M falls towards V_{th2} close to zero, R_M switches back from R_{on} to R_{off}. After $I(t)$ decreases to zero, the membrane potential settles at V_{rest}. If a non-volatile memristor is used, then the

DC E_{rest}-source must be supplemented by simply adding a reset voltage pulse as will be experimentally demonstrated in subsequent sections.

Although the selector has nonlinear $I-V$ characteristics, its R_{on} and R_{off} values are approximated to 0.7 MΩ and 10 MΩ for a tractable analysis. For $C = 0.1$nF, $I_0 = 20$nA, $V_{\text{threshold}} = -48$mV, $V_{\text{rest}} = -70$mV, and $E_{\text{rest}} = -70$mV, by the equation in (7) $t_{\text{clamp}} = 0.12$ms is estimated, which is close to the rise time of $V(t)$ from -70mV to -48mV in Fig. 3(d).

The operation of the MIF model is analyzed by using the following equations. Initially, the membrane potential $V(t)$ is at V_{rest} and the memristor in its R_{off} state. Upon receiving a positive input current $I(t)$, $V(t)$ increases with a time constant of $R_{\text{off}}C$. When $V(t)$ reaches $V_{\text{threshold}}$, the memristor switches to the on state, the capacitor starts discharging, and $V(t)$ decreases with a time constant $R_{\text{on}}C$. The relationship between $V(t)$, the voltage across the memristor V_M, and the DC voltage source E_{rest} is

$$V(t) = E_{\text{rest}} + V_M \tag{8}$$

Assuming a positive set-voltage $V_{\text{th1}} > 0$, and that the MIF circuit depolarizes at the time instant when the memristor is set, $V(t)$ increases to $V_{\text{threshold}}$ and (8) can be rewritten as

$$V_{\text{threshold}} = E_{\text{rest}} + V_M \tag{9}$$

For memristance switching to occur, the following limitation is imposed upon the memristors set voltage V_{th1}:

$$V_{\text{th1}} < V_{\text{threshold}} - V_{\text{rest}} \tag{10}$$

For example, with $V_{\text{threshold}} = -48$ mV and $E_{\text{rest}} = -70$ mV, the memristor set voltage V_{th1} should be lower than 22 mV. Alternatively, if a memristor has a set voltage V_{th1} of 20 mV, then for the same $V_{\text{threshold}} = -48$ mV, $E_{\text{rest}} < -68$ mV must be adjusted accordingly, with additional margins depending on the type of memristor used.

1) Minimality of the MIF Model: The MIF model is universally minimal in terms of the number of circuit elements and the integration area because no other model simpler than the MIF model composed of two passive elements, C and memristor, and a DC voltage source E_{rest}, can reproduce a spiking waveform featuring the two voltage levels, V_{rest} and $V_{\text{threshold}}$. The MIF circuit can also generate oscillatory spiking signals for a locally active memristor with S-shaped I-V characteristics under appropriate DC input current.

The MIF model with a locally active memristor can be driven to switch on and off continually, due to the dynamics of the membrane potential, thus generating oscillations under a DC current stimulus. In the MIF circuit, even with a locally and globally passive memristor, a spiking voltage is generated by the memristor's resistance (R_M)-switching controlled by the charge build-up on the capacitor, which raises the memristor voltage V_M to the set-voltage V_{th1}, and switches R_M to R_{on} for discharging with a fast time constant. If the memristor is volatile, it is autonomously reset after its recovery time and reaches its lowest level V_{rest}, reducing the memristor voltage V_M to V_{rest} - E_{rest} allowing the cycle to repeat, with the next voltage spike generated by the MIF circuit when a subsequent input current pulse turns the memristor on again. Even when the input current is DC, the MIF circuit with a locally active memristor can autonomously generate an oscillatory spiking output voltage waveform, which is comparable to the generalized LIF model with additional control circuitry depicted in Fig. 2(d). It should be noted that the MIF circuit does not require any additional control circuit. For instance, in the neuristor, featuring a topology based on the MIF circuit, the use of a locally active memristor with S-shaped $I_M - V_M$ characteristics has been used for the generation of oscillatory spikes under DC input current [47].

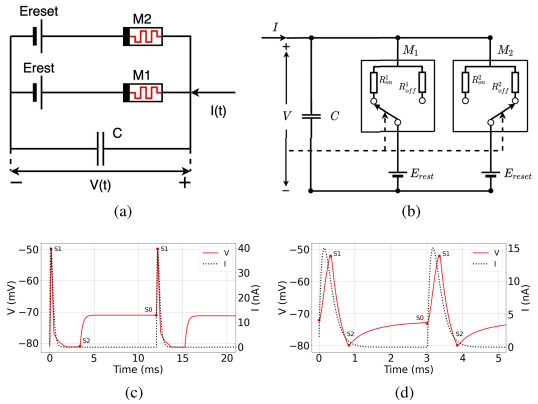

Fig. 4. The memristive integrate-and-fire neuron model: version 2. (a) MIF2 model with two memristors and two DC voltage sources. E_{rest} and E_{reset} correspond to E_{Na} and E_K in Fig. 1(a), respectively. (b) An illustration of the MIF2 circuit, in which V controls the resistance of both memristors. (c) Spectre simulation results using the model from Fig. 3. (d) Spectre simulation after tuning the MIF2 model parameters.

When a non-volatile memristor is used, as explained earlier, the DC E_{rest}-source must be supplemented at an appropriate time instant by an additive narrow voltage pulse of negative amplitude with a magnitude larger than $|V_{\text{th2}}|$, where V_{th2} is the negative reset-voltage of the non-volatile memristor. This point will be illustrated later through an experimental verification. No simpler circuit can produce such an action potential. Prior works require circuits with much more complex circuitry. Furthermore, a memristor consumes a smaller layout area as compared to a large resistor (Fig. 2(a)).

B. MIF2 Neuristor

In the typical waveform of the action potential from Fig. 1(c), the action potential $V(t)$ starts at V_{rest}, rises to $V_{\text{threshold}}$, resets to $V_{\text{reset}} < V_{\text{rest}}$, and settles at V_{rest}. It traverses three critical voltage levels. The need for a sub-rest voltage level stems from the refractory period during neuronal information transmission. Hyperpolarization suppresses the impact of an incoming stimulus to the neuron during the refractory period, and by driving the neuron to a voltage below the rest potential, it effectively raises the relative threshold, which the membrane capacitance voltage needs to attain for the generation of an action potential. While this may seem counterproductive, it prevents any stimulus already sent through the axon from triggering a backpropagating action potential to the neuron body. Therefore, hyperpolarization assures unidirectional signal transmission.

The MIF model in Fig. 3(a) cannot simulate all three transitions between V_{rest}, $V_{\text{threshold}}$ and V_{reset}. Another voltage source E_{reset} is required. Therefore, we propose the MIF2 model shown in Fig. 4(a-b). The use of a second memristor in series with a DC voltage source E_{reset} is derived from circuit-theoretic analysis and area density considerations. The MIF2 circuit is experimentally verified in the following sections, which demonstrates the generality of the new memristor-based neuron design.

TABLE I
PHASE TRANSITIONS OF THE TWO MEMRISTORS

Transition Phase of V(t)	M_1 (E_{rest})	M_2 (E_{reset})	Switching State
V_{rest} - $V_{threshold}$	off	off	S0
$V_{threshold}$ - V_{reset}	off	on	S1
V_{reset} - V_{rest}	on	off	S2

Topologically, the model is identical to the reduced HH model in Fig. 1(b) with $G_L = 0$ S [33]. The two DC voltage sources, $E_{\rm rest}$ and $E_{\rm reset}$, correspond to the $E_{\rm Na}$ and $E_{\rm K}$ voltage sources in the HH model. The current paths through the two memristors correspond to the $G_{\rm K}$ and $G_{\rm Na}$ channels in the HH model. In this regard, the MIF2 circuit can be considered a macro-model of the reduced HH model. This observation is consistent with the sequential opening of voltage-gated Na^+ and K^+ channels during action potential generation [51]. To summarize, the MIF2 circuit is devised so as to accurately reproduce the analog waveform of an action potential, and to capture the main mechanisms behind the generation of a biological neuronal spike.

The following equation describes the MIF2 model, where R_{M1} and R_{M2} denote the resistances of the memristors connected to $E_{\rm rest}$ and $E_{\rm reset}$, respectively:

$$C\frac{V(t)}{dt} = -\frac{V(t)-E_{\rm rest}}{R_{M1}(x_1, V(t))} - \frac{V(t)-E_{\rm reset}}{R_{M2}(x_2, V(t))} + I(t). \quad (11)$$

Equation (11) is valid through each of the three phases of action potential waveform. As $V(t)$ goes through different stages, the state $x_{i,j=1,2}$ of one of the two memristors may change accordingly. The key transitions in the capacitor voltage are: (1) $V_{\rm rest} - V_{\rm threshold}$, (2) $V_{\rm threshold} - V_{\rm reset}$, and (3) $V_{\rm reset} - V_{\rm rest}$. In each phase of the waveform $V(t)$ shown in Fig. 4(c) and (d), memristor M_1 (M_2) may switch between the off-resistance state and the on-resistance state, depending upon the bias voltage across it, i.e., the difference between $V(t)$ and the DC voltage level $E_{\rm rest}$ ($E_{\rm reset}$). Table I summarizes the state changes of the two memristors. To transition to the resting state, M_1 must be on to pull-up the potential by $E_{\rm rest}$.

An intuitive description of the operation is as follows. Assume M_1 and M_2 are both initially off. For the transition at $S0$, an input current injection $I(t)$ is applied, causing charge to build up on the capacitor. For a sufficiently large input, the voltage will reach the peak of the action potential which is also the point at which M_2 switches on. Note that the reset potential is more negative than the rest potential, which means the voltage drop across M_2 is greater than that across M_1. For identical memristors, M_2 will switch on first. This provides a low resistance pathway for the capacitor discharge. Thus, $V(t)$ will suddenly drop toward $E_{\rm reset}$. This corresponds to the transition phase associated to the switching state $S1$. If M_2 is a volatile memristor, then it will autonomously turn off causing $V(t)$ to relax back to the same value as in $S0$, which can be set to approximately $E_{\rm rest}$ if $R_{M1} \ll R_{M2}$. Alternatively, as in our experiments, M_2 may be a non-volatile memristor. A step pulse would then be applied at $E_{\rm reset}$, causing M_2 to switch off which has the same effect. This corresponds to the evolution along the transition phase $S2$. After the peak potential at $V_{\rm threshold}$ the membrane potential hyperpolarizes down to $V_{\rm reset}$. At reset, the membrane potential $V_{\rm reset}$ is constrained by the DC reset potential $E_{\rm reset}$ and the potential V_{M2} across the memristor M_2:

$$V(t) = V_{\rm reset} = E_{\rm reset} + V_{M2} \quad (12)$$

For the memristor M_2 to reset, the voltage across it must be less than $V_{\rm th2}$. Thus, the following constraint is imposed:

$$V_{\rm th2} > V_{\rm reset} - E_{\rm reset} \quad (13)$$

In the next phase, the membrane potential rises toward $V_{\rm rest}$ from $V_{\rm reset}$. The memristor M_2, connected to the voltage source $E_{\rm reset}$, is off ($R_{M2} = R_{\rm off}$), which prevents M_2 from blocking the pull-up effort from M_1 to raise $V(t)$ toward $E_{\rm rest}$.

An autonomous spiking behaviour can be achieved using volatile memristors appropriately biased via DC voltage sources and choosing a proper value for the membrane capacitance. Analytical expressions in the form of (6)–(7) can be derived for the MIF2 circuit with piecewise linear segments, but for analysis with more realistic nonlinear $I-V$ characteristics, Cadence/Spectre simulation is used. The simulation results are shown in Fig. 4(c). $V(t)$ rises to the peak value, dips to $V_{\rm reset}$, and then rises to $V_{\rm rest}$, which is behaviorally correct. As qualitatively described earlier, in its dynamical evolution $V(t)$ goes through three distinct voltage levels, namely $V_{\rm threshold}$, $V_{\rm reset}$, and $V_{\rm rest}$, as governed by the resistance switching phenomena occurring in the two memristors, and indicated in Fig. 4(c) by $S0$, $S1$, $S2$, defined in Table I to denote the memristors' resistance states along the three distinct transition phases of the membrane capacitance voltage.

Some circuit parameters can be tuned to slow down the phase transitions of the capacitor voltage $V(t)$, as shown in Fig. 4(d), which displays a spiking voltage waveform strikingly similar to that in Fig. 1(c). In this case, the memristor M_1 remained in the off state at all times. For the case using non-volatile memristors in the MIF2 circuit, a narrow voltage pulse should be added to the voltage source $E_{\rm reset}$. This will be discussed in the experimental section. Fig. 4(d) shows simulation results of the MIF2 circuit for the case where M_1 and M_2 are identical volatile memristors. The two DC voltage sources can be tuned to mimic the action potential waveform closely. Setting $E_{\rm reset}$ and $E_{\rm rest}$ to -80 mV and -65 mV, respectively, the membrane potential displayed a rest potential of -72.5 mV, and a reset potential of -80 mV. For $V_{\rm threshold} = -52$ mV, the memristor M_1, connected serially to the $E_{\rm rest}$-battery, remains in the off-state.

1) Minimality of the MIF2 Model: The MIF2 model consisting of one capacitor, and two memristors M_1 and M_2, connected to DC voltage sources $E_{\rm rest}$ and $E_{\rm reset}$, respectively, is minimal in terms of number of circuit elements and integration area in generating a spiking neuronal signal waveform with three voltage levels, specifically $V_{\rm rest}$, $V_{\rm threshold}$, and $V_{\rm reset}$. The MIF2 circuit with locally active memristors can generate oscillatory spiking signals under sufficient DC input current.

The MIF2 model resembles the memristive HH model with battery-driven sodium and potassium ion channels. The MIF2 circuit is topologically equivalent to the reduced memristive HH model when compared to Fig. 1(a), neglecting leakage terms [33]. The DC voltage sources, $E_{\rm rest}$ and $E_{\rm reset}$, in the MIF2 circuit represent the rest and reset potentials, and correspond to the batteries $E_{\rm Na}$ and $E_{\rm K}$ in the HH model. Previously, it was shown that for the generation of a membrane potential waveform which does not dip to $V_{\rm reset}$, the proposed MIF circuit in Fig. 3(a) is minimal in terms of number of circuit elements and integration area. To model hyperpolarization, the inclusion of an additional battery-driven memristive pathway is necessary. Otherwise, the drop to the $V_{\rm reset}$ level cannot be replicated without external control circuitry [34]. Although a resistor may be chosen in lieu of a memristor

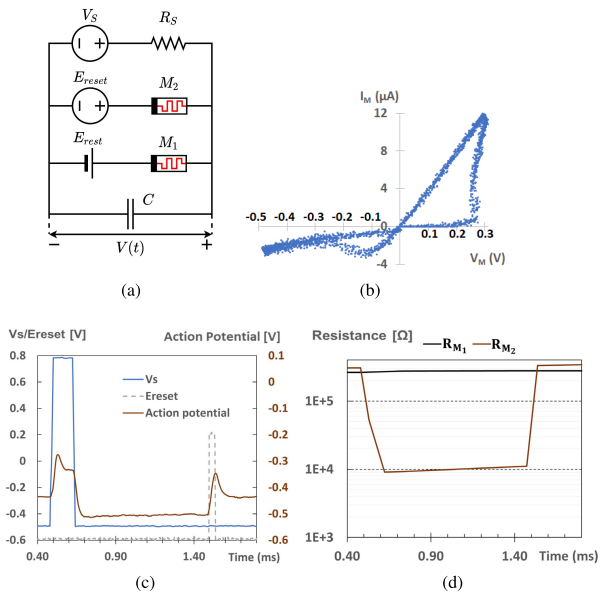

Fig. 5. Experimental results of the MIF2 circuit using Knowm memristors. (a) MIF2 circuit, including a parallel path with a voltage source and its series resistance providing the stimulus current ($I(t)$ in Fig. 4(a)). (b) $I-V$ characteristics of the Knowm memristor used for experimental verification of the MIF2 model. (c) Measured action potential waveform of the MIF2 circuit. The action potential signal corresponds to membrane potential $V(t)$. (d) Time evolution of the resistances of memristors, R_{M1} and R_{M2}, during action potential generation.

to generate a new voltage level, such a choice may not preserve the MIF2 minimality in terms of integration area, and furthermore, does not allow the replication of the $I-V$ characteristic of the reset memristive path with an AC driving stimulus, which is a signature peculiar to resistance switching memories. The two memristors in the MIF2 model can be volatile or non-volatile. The E_{rest} and E_{reset} sources can be purely DC for the case of volatile memristors. If a non-volatile memristor is used as M2, a reset pulse must be added to E_{reset}. This point will be further described in the next experimental section where commercially available, non-volatile memristors are used to emulate spiking neuronal signal generation.

IV. Experimental Results

We first show our experimental results using low-cost commercially available Knowm memristors to demonstrate generality. Although alternative devices may be better suited for use in the MIF family of neuron models, the Knowm devices are selected due to their accessibility.

A. Experimental Setup

Our experimental setup used Knowm memristors with a tungsten W + Ge_2Se_3 active layer in discrete form. The values of R_{on} and R_{off} were measured to be 22 kΩ and 320 kΩ, while $V_{\text{th1}} = 0.28$ V and $V_{\text{th2}} = -0.2$ V at room temperature. This memristor exhibited non-volatility within the timescales of the experiment. Two memristors from the same batch, with the $I_M - V_M$ characteristic curve shown in Fig. 5(b), were adopted for testing the MIF2 circuit in Fig. 5(a) under an input voltage pulse V_S of width T_W connected in series with a source resistor R_s, in lieu of an ideal current source. Under this stimulus, the membrane potential $V(t)$ starts from V_{rest} and increases to $V_{\text{threshold}}$ within a period of t_{clamp}, and then falls to V_{reset} within a period of t_{fall} as shown in Fig. 5(c). The time evolution of the resistances of each of the two memristors is depicted in Fig. 5(d), showing how the resistance of M_2 fluctuates around the constant resistance of M_1. The voltage across the memristor M_1, $V(t) - E_{\text{rest}}$, should be such that M_1 remains in its off state, which imposes a constraint on the value of $V_{\text{threshold}}$. The state equation of the MIF2 circuit in Fig. 5(a), where the current in (11) is derived out of the equivalent voltage-driven Thevenin circuit, shown in (14). From the time instant when $V(t)$ is equal to V_{rest} until the time instant when $V(t)$ is equal to $V_{\text{threshold}}$, the resistance of M_2 is $R_{2\text{off}}$ and the resistance of M_1 is $R_{1\text{off}}$, V_S has a magnitude of V_{sp}, thus the circuit equation becomes

$$C\frac{V(t)}{dt} = -\frac{V(t)-E_{\text{rest}}}{R_{1\text{off}}} - \frac{V(t)-E_{\text{reset}}}{R_{2\text{off}}} + \frac{V_{\text{sp}}-V(t)}{R_S} \quad (14)$$

Equation (14) can be solved to find t_{clamp} as

$$t_{\text{clamp}} = R_{\text{eq1}} C \ln\left(\frac{V_{\text{f1}}-V_{\text{rest}}}{V_{\text{f1}}-V_{\text{threshold}}}\right) \quad (15)$$

$$V_{\text{f1}} = R_{\text{eq1}}\left(\frac{V_{\text{sp}}}{R_S} + \frac{E_{\text{reset}}}{R_{2\text{off}}}\right) \text{ and}$$

$$\frac{1}{R_{\text{eq1}}} = \frac{1}{R_S} + \frac{1}{R_{1\text{off}}} + \frac{1}{R_{2\text{off}}} \quad (16)$$

R_{eq1} is the equivalent resistance of three resistors in parallel as shown in (16), V_{sp} is the peak voltage value of the voltage source V_S (+0.8V), V_{f1} is the steady state membrane potential $V(t)$ when the voltage source peak value V_{sp} is sustained for a long duration, and $E_{\text{reset}} = -0.60$ V. Through a fitting procedure using the measured values for the reset and set membrane capacitance voltages V_{rest} and V_{reset}, we determined the effective resistance values of the memristors in operation as: $R_{1\text{off}} = 264\text{k}\Omega$, $R_{2\text{off}} = 307\text{k}\Omega$, $R_{2\text{on}} = 9.8\text{k}\Omega$. These values are not exactly same as the values measured in the stand-alone devices.

B. Experimental Analysis of the MIF2 Circuit

Fig. 5(c) shows the measured action potential waveform of the MIF2 circuit employing two memristors with measured $I_M - V_M$ characteristics as shown in Fig. 5(b) and driven by a voltage source in series with a resistor.

Although not identical to the simulated result in Fig. 4(c–d), the action potential waveform displays 3 distinct voltage levels: V_{rest}, $V_{\text{threshold}}$, and V_{reset}. An overshoot can be observed during the reset pulse before $V(t)$ settles to V_{rest}. An analysis is provided below on how this overshoot can be removed by tuning ad hoc circuit parameters. Fig. 6(a) illustrates the time course of the membrane capacitance voltage, which exhibits an overshoot as a reset pulse of amplitude $E_{\text{reset-p}}$ is superimposed on the E_{reset} level. The overshoot is observed during the time interval when the reset pulse allows to restore M_2 to the off sate. Here, M_1 was found to remain in its off state at all times. The recovery time, t_{rec}, represents the time interval between the instant t_A at which the action potential starts to rise from the reset voltage level, i.e., the instant which the reset pulse-based stimulation of M_2 commences, and the instant t_B at which the action potential attains the rest voltage level. In order to suppress the overshoot in the membrane capacitance voltage during the pulse stimulation, which resets to M_2, the recovery time should be smaller than an upper bound, as computed via (17)–(19). $E_{\text{reset-p}}$ denotes the reset

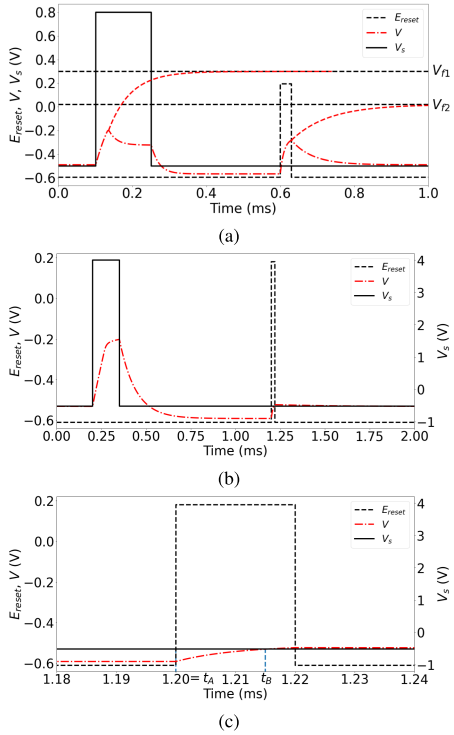

Fig. 6. LTSpice simulation of the MIF2 circuit using the Knowm memristor model. (a) Time waveforms of E_{reset}, V_S, $V(t)$. In the event the pulse V_S (E_{reset}) is infinitely long, the temporal trace, which $V(t)$ would exhibit after such AC stimulus, would rise asymptotically to V_{f1} (V_{f2}). (b) Removal of the overshoot in $V(t)$ with larger capacitance (10 nF vs. 1 nF) and source voltage (4 V vs. 0.8 V). (c) Graphical indication of t_A and t_B on the time axis in an enlarged view of plot (b) over the phase when M_2 is reset to the off state.

pulse amplitude. Note that in (17) and (19), $R_{2\text{off}}$ is replaced with $R_{2\text{on}}$ to account for the off-to-on state transition induced in M_2 by the pulse amplitude $E_{\text{reset}-\text{p}}$ superimposed on the baseline of the signal generated by the source E_{reset}.

$$C\frac{V(t)}{dt} = -\frac{V(t)-E_{\text{rest}}}{R_{1\text{off}}} - \frac{V(t)-E_{\text{reset}}}{R_{2\text{on}}} + \frac{V_S - V(t)}{R_S} \tag{17}$$

$$t_{rec} \leq t_B - t_A = R_{eq2}C\ln\frac{V_{f2}-V_{reset}}{V_{f2}-V_{rest}} \tag{18}$$

$$\frac{1}{R_{eq2}} = \frac{1}{R_S} + \frac{1}{R_{1off}} + \frac{1}{R_{2on}};$$

$$V_{f2} = R_{eq2}\left(\frac{V_S}{R_S} + \frac{E_{rest}}{R_{1off}} + \frac{E_{reset-p}}{R_{2on}}\right) \tag{19}$$

where R_{eq2} is the equivalent resistance of three parallel resistors, specifically R_S, R_{M1}, and R_{M2}, when $E_{\text{reset}}(t) = E_{\text{reset}-\text{p}}$, V_{f2} is the level the membrane capacitance voltage $V(t)$ would attain asymptotically if E_{reset} was held equal to $E_{\text{reset}-\text{p}} = 0.20$ V for all time after t_A. The input source voltage V_S is set at -0.50 V. To remove the overshoot in $V(t)$ during the procedure implemented to reset M_2, we can increase both the capacitance and the amplitude of the pulse superimposed on the baseline of the voltage source V_S to allow the transition of the membrane capacitance voltage from V_{rest} to $V_{\text{threshold}}$. The simulation result shown in Fig. 6(b) with a larger capacitance (10nF) and a higher value assigned to V_S during the transition of $V(t)$ from V_{rest} to $V_{\text{threshold}}$ (4 V) results in the complete suppression of the overshoot in the membrane capacitance voltage. The maximum allowable recovery time to suppress the voltage overshoot is calculated using (18), and amounts to 10.9 μs, which is comparable to the LTspice-simulated value of 14.8 μs in Fig. 6(c).

TABLE II

IMPACT OF THE VOLATILE MEMRISTOR DEVICE VARIABILITY ON THE RESET AND REST DYNAMICS OF THE MEMBRANE CAPACITANCE VOLTAGE IN THE MIF2 NEURISTOR (SECTION III.B)

Parameter	Variation	t_{reset}	t_{rest}
R_{on} 1kΩ	-20%	-4.7%	-5.6%
	20%	2.3%	5.4%
R_{off} 100kΩ	-20%	-2.4%	+2.8%
	20%	-0.9%	-0.5%
V_{th1} 110mV	-20%	-8.1%	-24.6%
	20%	9.3%	94.9%
V_{th2} 5mV	-20%	-1.1%	3.0%
	20%	-0.2%	-2.2%

In summary, we have experimentally verified that the MIF2 circuit allows the use of non-volatile memristors to generate action potential waveforms. To overcome the difficulties caused by the negative reset transition voltage in non-volatile memristors, the DC E_{reset} source is complemented with a pulse so that the combined voltage enables a transition of the membrane capacitance voltage $V(t)$ from V_{reset} to V_{rest}. Taking safe margins, the pulse amplitude should be chosen larger than the difference between $V_{\text{threshold}}$ and the sum of V_{th2} and the DC component of E_{reset}. This amplitude level needs to be sustained for a brief, but sufficient time, to enable the memristor M_2 to turn off (on the order of 10μs in our experiments), allowing $V(t)$ to attain the V_{rest} level before the next cycle may begin. The action potential, measured from the hardware prototype, features three noticeably distinct voltage levels, as shown in Fig. 5(c). Though it exhibits an overshoot phenomenon, the method for suppression that accompanies the reset procedure of M_2 has been detailed above.

C. Statistical Variation of Knowm Memristors

Another important consideration is the effect of statistical variation in key memristor parameters R_{on}, R_{off}, V_{th1} and V_{th2} on action potential signal generation. Statistical variations of ±20% were applied to these memristor parameters to explore the impact on the performances of the MIF2 electronic neuron model discussed in section III-B and IV, and employing volatile and non-volatile memristors, respectively. t_{reset} and t_{reset} are used as measures of the performance of the MIF2 neuristor from section III-B. Here, t_{reset} is the time it takes for $V(t)$ to descend from $V_{\text{threshold}}$ to V_{reset}, while t_{rest} denotes the time it takes for $V(t)$ to rise from V_{reset} up to the level amounting to $0.9 \cdot (V_{\text{rest}} - V_{\text{reset}})$. The impact of parameter variance using volatile memristors on set/reset variation is shown in Table II. $V_{\text{rest}} - V_{\text{reset}}$, the difference between the rest potential and the reset potential, is used as the measure of performance for the MIF2 neuristor with non-volatile memristors in Section IV, because the timing in the various phases, which the capacitance membrane potential undergoes during each spiking cycle, is dictated by the time waveforms of the voltage stimuli V_S and E_{reset}. The impact of the device variability on the performance of the MIF2 circuit with non-volatile memristors may be inferred from Table III.

V. DISCUSSION AND ANALYSIS

The pursuit for VLSI implementation of spiking neural networks dates back to Mead's early work [1] and has been expanded since then [52]. A highly compact physical implementation of the LIF neuron model was introduced by using a multitude of MOSFETs, resistors, and SCRs [53]. This section focuses on the most compact physical realization of the MIF

TABLE III

IMPACT OF THE NON-VOLATILE KNOWM MEMRISTOR VARIABILITY ON THE RESET AND REST DYNAMICS OF THE MEMBRANE CAPACITANCE VOLTAGE IN THE MIF2 NEURISTOR (SECTION IV)

Parameter	Variation	V_{rest} - V_{reset}
R_{on} 900Ω	-20%	-4.8%
	20%	-5.2%
R_{off} 15kΩ	-20%	5.0%
	20%	-4.0%
V_{th1} 180mV	-20%	-13.6%
	20%	-1.2%
V_{th2} -100mV	-20%	0.0%
	20%	0.0%

circuit model from Fig. 3(a) as well as its extension, the MIF2 circuit, from Fig. 4(a). As discussed earlier, the use of nanoscale memristors as neuristors allows the highest packing density in analog spiking neural network implementations as opposed to the use of resistors and other complex switching circuitry. Moreover, the impact of stimuli rate on the memristive dynamics in the proposed MIF and MIF2 neuron models cannot be reproduced if the memristors are replaced with resistors. Interestingly, our parameter sweep analysis shows that the memristor on and off resistance variability, which is typically the most critical source of concern, does not have a significant effect on cycle-to-cycle variability in the membrane capacitance voltage. On the other hand, the reset and rest times are highly sensitive to the threshold voltage $V_{\rm th1}$. This provides insight to device researchers that reducing the variability in the set threshold voltage $V_{\rm th1}$ of either volatile or non-volatile memristors may prove to be the decisive factor improving the cycle-to-cycle repeatability of the dynamical phenomena emerging in neuristors.

A. VLSI Implementation of a Memristive Solid-State Brain

An idealization of the neuron is shown in Fig. 7(a) as part of a general network representation [54]. A layout of the MIF2 neuron with a fan-out of three synapses is shown in Fig. 7(b). The vertical metal line has a finite bit-line capacitance $C_{\rm bit}$. This vertical line also sources the input current I_1.

The resulting potential along the vertical line is the membrane capacitance voltage V_{c1} of the MIF2 neuristor. $M_{\rm rest1}$ is the memristor in series with $E_{\rm rest}$, while M_{1-j}, $j = 2, 3, 4$, is the synaptic memristor between the axon terminal connected to neuron 1 and the j^{th} post-synaptic neuron, not shown here. Memristors are formed vertically at the cross-points. This layout shows that the entire neuronal network in Fig. 7(a) can be laid out in a single column, thus taking up a small area, which translates into a high on-chip packing density. More complex neural networks can be implemented in a vertically stacked 3D structure as in the brain. For the layout of the MIF2 circuit, a thin horizontal line for $E_{\rm reset}$ is inserted next to the $E_{\rm rest}$-line, or vertically above it. It is possible to level-shift both DC sources such that one is fixed to ground to reduce biasing requirements [44], [55]. The voltage difference between the two sources can give rise to second-order effects that act on longer time scales than action potentials, such as spike frequency adaptation. While it introduces additional overhead, sharing biases across neurons can allow the MIF and MIF2 circuits to draw advantages from continued scaling. In the following sub-sections, a simple analysis of a solid-state brain composed of MIF neuristors, in terms of surface area and power consumption will be presented.

Emulating biological neurons with a high fan-out in silicon has been a long-standing challenge over the past few decades.

TABLE IV

MEMRISTIVE NEURON COMPARISON

Memristive Model	No. Elements	Refractory Period	Reset Dynamics	Energy p/Spike
MIF1	2 (3)	No	No	4.9 pJ
MIF2	3 (5)	Yes	Yes	12.8 pJ
Neuristor [47]	8	Yes	Yes	417 pJ
Zhang *et al.* [44]	4	No	No	12 μJ
Lin *et al.* [56]	4	No	No	NA
Stoliar *et al.* [57]	3	No	No	NA
Wang *et al.* 1 [58]	2	No	No	NA
Wang *et al.* 2 [59]	3	No	No	NA

The large capacitive loading of the op amps employed in the neuron circuits reduces their slew rate, although is not a major issue where phenomena acting over slow biological timescales are reproduced. Rather, the most critical issue is signal attenuation. As an example of a neuronal circuit with high fan-out, we have simulated an artificial neural network consisting of three layers of MIF2 neuristors connected one to the other via synapses. The circuit topology is shown in Fig. 7(e), where $R_I = 0.1\text{K}\Omega$ and $\text{R}_{\text{syn,a}-\text{b}} = 1\text{K}\Omega$ where $a - b = \{1-2, 2-3\}$. For simplicity, we use a linear resistor in place for the synapses. The second layer is set to drive 30 neurons through synaptic connections, which are preceded by a voltage follower used to buffer the spike coming from the single pre-synaptic MIF2 neuristor. The follower is effectively used as a voltage-controlled voltage-source (VCVS), which mimics the chemically-driven propagation of an action potential along the axon of the pre-synaptic MIF2 neuristor [51].

SPICE simulations of the MIF2 neuristor-based fully-connected network without buffering is shown in Fig. 7(c). Signal attenuation in the deeper layer is drastic, which motivates the decoupling of the intermediate MIF2 circuit from the 30 neuristors it is synaptically connected to using a buffer. In many spiking networks, the spike timing rather than its waveform is the mechanism for neural encoding. In such cases, a simple digital spike read out circuit which would be typically implemented by a current-mode sense amplifier (or alternatively, with an ad hoc arrangement of cross-coupled inverters) [60]. However, in case the spike analog waveform encoded neural information, its propagation to a large number of post-synaptic neurons would require a buffer, as shown in the illustrative example of Fig. 7(e), the simulation of which is depicted in Fig. 7(d). Signal integrity is maintained through 3 layers of MIF2 neurons, even without buffering between the first and second layers. The total dynamic power of the network of Fig. 7(e) is shown with the dashed line in Fig. 7(c). The capacitance of each neuron's capacitor is 1 pF. The total energy dissipated in the network is 436 pJ, which corresponds to an energy per neuron of 12.8 pJ, and power consumption per neuron of 12.8 pW under 1 Hz operation as the network uses 34 neurons. The buffer consumes 164 pW (4.82 pW/neuron), which is 38% of the total power consumed by the network. A performance comparison between the proposed MIF and MIF2 neuron designs and other key memristive neuron designs is provided in Table IV.

The number of elements refers to those that are unshared across neurons, with those in parentheses including the DC sources of the MIF and MIF2 neurons. Refractory period refers to whether the neuristor has a depolarization (or some other homeostatic) mechanism driving the membrane potential below the resting state. The reset mechanism refers to whether a membrane potential reset has been included to drive the neuron back to its resting potential, such as switching M_2 off

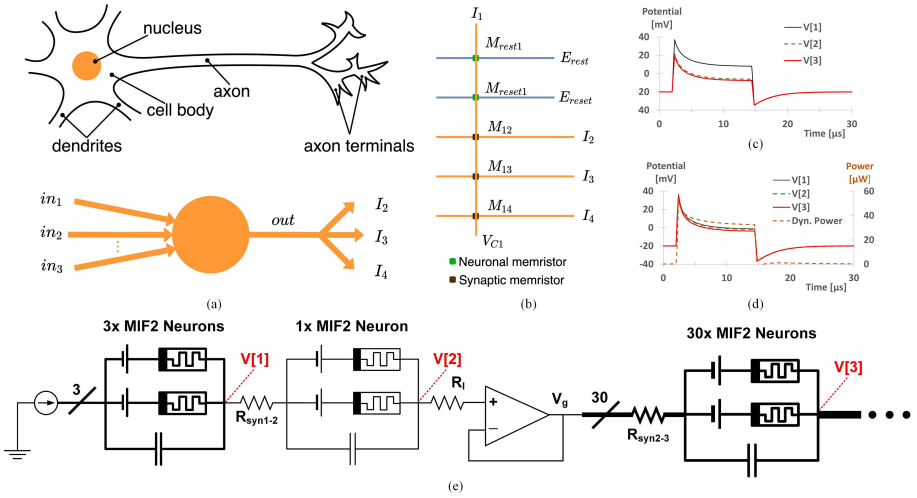

Fig. 7. Neural network implementation using the MIF2 model and synaptic resistors (R_{syn1-2} and R_{syn2-3}). (a) A simple neuronal network with both fan-in and fan-out equal to three each. (b) Layout of the neuronal network in (a). V_{c1} is the voltage across the membrane capacitance in the MIF2 circuit excited by I_1. I_{2-4} are the fan-out currents of the neuron circuit. (c) Simulation result of (e) without buffering, showing that loading from subsequent stages attenuates the spike amplitude. $V[1]$, $V[2]$, and $V[3]$ denote the output voltage of each subsequent stage, i.e., the 1st, 2nd and 3rd neural layer, respectively. (d) Simulation results of (e) with buffering showing that high fan-outs are possible due to the high input/low output impedance of the voltage follower. (e) Circuit topology of MIF2-based neuronal network with a high fan-out of 30 using a voltage follower interposed between neurons and synapses which maintains signal integrity. Each synapse $R_{\text{syn},2-3}$ shares the left terminal only. A voltage buffer is necessary for large fan-out, as is depicted in the third MIF stage. In the brain, each neuron may have a fan-out of anywhere from 1,000–10,000, which would demand buffers between all stages.

in the MIF2 circuit with non-volatile memristors (section IV). We estimated the energy consumed by a neuron per spike, and several other power consumption metrics, on the basis of the data provided in [47] and [44]. A row with label 'not applicable (NA)' refers to a neuristor design which did not include the performance measure.

Additionally, if we consider the design of a sparsely connected spiking neural network, a typical neuron has a similar number of input and output synaptic connections, which creates balanced fan-in and fan-out characteristics. Taking into account the relatively low frequency spiking nature of neurons, the necessary buffer circuitry has relaxed design considerations to ensure signal integrity through a deep network.

B. Brain vs. Memristive Solid-State Implementation: Surface Area Comparison

In view of a future implementation of a solid-state brain composed of MIF2 neurons, synapses, and interconnects, this section benchmarks its surface area against the human brain counterpart [61].

- Number of neurons = 10^{11}
- Number of synapses = 10^{14} – 10^{15}
- Median surface area = 2,400cm^2
- Median volume = 1,050 cm^3

Fig. 7(b) indicates that each neuron and each synapse can be laid out using the same area, amounting to $4F^2$, where F represents the minimum feature size for the width of horizontal and vertical lines used in the crossbar array. For instance, at the 5nm fabrication technology node (F = 5nm) with minimum pitch of $2F$, an area of $4F^2$ is required for a neuron or a synapse. Based on state-of-the-art reports on VLSI implementations of neuromorphic circuits, it can be conservatively assumed that, due to hardware overhead necessary to accommodate interconnects, sensing and peripheral circuitry, as well as to meet additional requirements, the area allocated to each neuron and synapse is set to $5{\cdot}4F^2$ [62], [63]. Thus, each instance of a neuron or a synapse has an area of $20F^2$ allocated on chip as a conservative estimate. In a simple estimation, the total area required to realize all neurons, synapses, DC voltage source lines, and ground lines, in a future realization of a memristive solid-state brain, is:

- Area = $20F^2 \times (10^{11} + 10^{15})$
- For F = 5nm, the area required would be: $20 \times (5 \times 10^{-9})^2 \times (10^{11} + 10^{15})$ = 5,000cm^2

By comparison, physiologically, the median surface area of the brain is 2,400cm^2, which is smaller by a factor of 2.1. On the other hand, with F = 3.5nm, the surface area of the human brain and of its envisioned solid-state implementation become approximately the same. Thus, memristor technology integrated through a fabrication process with an aggressive scaling target, can potentially enable the circuit realization of a solid-state brain within a surface area equivalent to the biological human brain one. If the need for more complex circuitry demanded the availability of additional chip area, multiple stacked layers could be used so as to prevent any further enlargement of the surface area. Since the biological brain has a 3D structure, the memristive solid-state brain can also be constructed vertically across a dozen stacked layers, stretching across a thickness of approximately 0.3 cm, close to the physiological thickness of the median cortical sheet, in which 1,050cm^3 / 2,400cm^2 = 0.44 cm.

C. Brain vs. Memristive Solid-State Implementation: Power Comparison

This section benchmarks the power consumption of the memristive solid-state brain against the human brain counterpart. With reference to the artificial realization, we need to evaluate the power of each neuristor, of each synaptic element, and of each wire connecting any two components in each layer. Considering MIF neurons for simplicity, the average power consumption per neuron can be estimated as follows. First, the average power dissipated in the MIF circuit as the capacitance membrane potential $V(t)$ builds up from V_{rest} to $V_{\text{threshold}}$ over the charge-up period t_{clamp} is computed via

$$P_{\text{clamp}} = \frac{1}{t_{\text{clamp}}} \int_0^{t_{\text{clamp}}} I(t)V(t)\text{dt} \tag{20}$$

It is estimated that the human brain, composed of about 10^{11} neurons and 10^{15} synapses, consumes a power oscillating between 12 and 20 W [64]. An order of magnitude for the power dissipated by the brain may be estimated through the following formula, in which n represents the number of synapses per neuron:

$$\begin{aligned} P_{\text{brain}} &= N_{\text{neurons}} \times n \times V_{\text{spikes}} \times I_{\text{spike}} \times T_{\text{period}} \times f_{\text{spike}} \\ &= 10^{11}\text{neurons} \times 10^{4}\text{syn/neuron} \times 10^{-1}\text{V} \\ &\quad \times 10^{-10}\text{A} \times 10^{-3}\text{sec} \times 1\text{Hz} \\ &= 10\text{W} \end{aligned} \tag{21}$$

More precisely, calculations based on caloric intake place the upper ceiling estimate at 23.3W [65], and the floor estimate at 12.6W [66], which leads to the often-cited 20W value for the human brain power. A simple calculation of the power consumed per spike by each neuron or synapse gives P_n = 10fW. With reference to section III.A, in order for a MIF circuit to consume a power per spike with an order of magnitude of fW, a small value, in the pA range, needs to be assigned to I_0. The current can be increased significantly if the brain power is assumed to depend mainly on the neuron power consumption. Then, the power budget per neuron can be increased by a few orders of magnitude.

As an illustrative example, let us set the MIF circuit parameters as follows: R_{off} = 50 GΩ, C = 0.1 pF, E_{rest} = −70mV, V_{rest} = −60mV, $V_{\text{threshold}}$ = 30mV, and I_0 = 2.5pA. We find $\tau = R_{\text{off}}C$ = 5ms and t_{clamp} = 7.63 ms from (7).

In a simpler analysis to be used next, with $V(t)$ approximated using a triangular function, P_{clamp} can be estimated via

$$P_{\text{clamp}} = I_0 \frac{V_{\text{threshold}} - V_{\text{rest}}}{2}, \tag{22}$$

which is then numerically evaluated as 2.5pA × 0.5(30 + 60) mV = 112.5fW. The average power $P_{\text{discharge}}$ dissipated by the MIF circuit as the capacitance membrane voltage $V(t)$ descends from $V_{\text{threshold}}$ back to V_{rest} would be smaller than P_{clamp} by at least one order of magnitude, since the memristor resistance is R_{on} during the capacitance discharge phase, and R_{on} is lower than R_{off} by at least one order of magnitude. Thus, the average power consumption P_n of the MIF neuristor over the temporal duration T_{period} of one action potential is

$$P_n = P_{\text{clamp}}(1 + R_{\text{on}}/R_{\text{off}})t_{\text{clamp}}/T_{\text{period}} \tag{23}$$

For the above example, if the temporal duration T_{period} of one action potential is 20 ms, and $R_{\text{on}}/\text{R}_{\text{off}}$ = 0.01, then by (23), P_n = 112.5fW × (1 + 0.01) × (7.63 ms / 20 ms) = 47.2 fW.

In practice, non-volatile memristors are often used to emulate synapses, while volatile devices with finite relaxation times are employed to emulate neurons. The total energy consumption per spike reported for the volatile memristor from [45] is approximately 50 fJ, which is comparable to the energy budget per action potential in a biological neuron [67]. If it is assumed that the average neuron firing rate is 1 Hz [68], then the total power consumed by the volatile memristor-based neuristor from [45] per spike is 50 fW, which closely matches the 47.2 fW value calculated from (23).

Let us now set the MIF circuit parameters as follows: R_{off} = 50 MΩ, C = 10 pF, E_{rest} = −70 mV, V_{rest} = −60 mV, $V_{\text{threshold}}$ = 30 mV, and I_0 = 2.5 nA. We would then obtain τ = 0.5 ms, and t_{clamp} = 0.763 ms. From (22), it would thus be P_{clamp} = 112.5 pW. Equation (23) would finally give P_n = 112.5 pW × 0.763 ms / 20 ms = 4.29 pW, which is higher by two orders of magnitude with respect to its value in the previous case, where I_0 was lower by three orders of magnitude. However, if neurons are assumed to dominate the power consumption, then a nA-range current for I_0 in the MIF circuit from section III.A would be considered reasonable. It can be stated that

$$P_n = f(I_0, C, R_{\text{on}}, R_{\text{off}}, E_{\text{rest}}, E_{\text{reset}}, V_{\text{rest}}, V_{\text{threshold}}).$$

To reduce power consumption, the voltage swing $V_{\text{threshold}} - V_{\text{rest}}$ should be kept small. $R_{\text{off}}I_0$ can be lowered accordingly, allowing a smaller I_0. This observation is useful for the design of memristive spiking neural networks, especially to specify memristor parameters (R_{on}, R_{off}, V_{th1}, and V_{th2}).

If all neurons are assumed to spike within a same temporal window of width T_{period} = 20 ms, then the total power consumption of neurons and synapses per spike period, $P_{n\&s}$, can be estimated via

$$P_{n\&s} = 47.2 \times 10^{-15}(10^{11} + 10^{15})W \approx 47.2W,$$

and therefore, the total energy $E_{n\&s}$ consumed by neurons and synapses per spike period T_{period} would amount to 47.2 W × 20 ms = 944 mJ.

The power consumed by neurons and synapses is estimated to be about 2/3 of the total brain power, while about half of $P_{n\&s}$ is consumed by interconnects. Thus, when all neurons and synapses are assumed to spike within a single window of period T_{period}, it is reasonable to compute the resulting power consumption P_{Brain} in the brain, where neurons emit a spike with an average probability of around 30%, as

$$\begin{aligned} P_{\text{Brain}} &= 0.3 \times 1.5 P_{n\&s} \\ &= 21.2W, \end{aligned}$$

which falls in the typical ballpark of 20 W.

VI. Conclusion

The introduction of the MIF and MIF2 neuron circuits is poised to enable the future hardware realization of disruptive bio-inspired spiking neural networks, featuring surface and volume dimensions and operating under power budgets comparable to the corresponding characteristics of a human brain, which displays a median surface area of 2,400 cm^2, a median volume of 1,050 cm^3, and consumes about 20W of power. Importantly, the proposed neuristor circuit-theoretic models, are general. In fact, the single (two) passive memristor (memristors) employed in the proposed MIF (MIF2) neuristor may be either volatile or non-volatile. The MIF2 neuristor and the reduced memristive Hodgkin-Huxley circuit [7] are topologically equivalent, and their parameters are physiologically comparable. The operating mechanisms of the MIF (MIF2) circuit are critically dependent upon the resistance switching phenomena emerging in its non-volatile or volatile memristor (memristors). As a result, the memristor fabrication process needs to be optimized toward the production of devices with stable off and on resistances and well-defined set and reset voltages. The variability of the memristor set threshold voltage proves to be the undesired effect, and is most deleterious to cycle-to-cycle repeatability of the action potential generation dynamics in the MIF2 circuit with either volatile or non-volatile resistance switching memories.

In case one (two) volatile and locally-active memristor(s) are employed in the MIF(2) circuit design, the resulting neuristor may even undergo sustained spiking oscillations under a DC input current of appropriate value. On the other hand, if a non-volatile memristor is employed in the design of either neuristor, an ad hoc pulse destabilization of the associated circuit over an appropriate time window triggers a train of action potentials across the membrane capacitance.

A hardware demonstration using off-the-shelf components, including a volatile memristor selector (two non-volatile Knowm resistance switching memories) showed that the MIF (MIF2) neuristor may generate spiking neuronal signals of similar shape as a biological neuron in the human brain. As shown through the analysis of a crossbar-based layout for coupling neurons via synapses, on-chip neural networks can be laid out compactly. It is estimated that, leveraging a 3.5 nm fabrication technology node, an entire solid-state brain, based upon a multi-layer memristive crossbar, could be laid out across a surface area and feature a vertical thickness comparable to the human brain median sizes.

The manuscript is concluded with a systematic estimation of the spiking power of a solid-state brain with MIF neuristors. With some simplifying assumptions, the total power, which the memristive brain is expected to dissipate, falls within the 20 W ballpark, which is frequently cited in the literature. The future realization of a memristive solid-state brain shall offer a tantalizing opportunity for further advancements in nanoscale memristor fabrication technologies. It will also pave the way toward the deployment of innovative brain-like computing machines with unprecedented performance capabilities in electronics, toward overcoming the modern challenges of large-scale data processing systems.

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REFERENCES

[1] C. Mead, "Neuromorphic electronic systems," *Proc. IEEE*, vol. 78, no. 10, pp. 1629–1636, Oct. 1990.

[2] D. Monroe, "Neuromorphic computing gets ready for the (really) big time," *Commun. ACM*, vol. 57, no. 6, pp. 13–15, Jun. 2014.

[3] M. Davies *et al.*, "Loihi: A neuromorphic manycore processor with on-chip learning," *IEEE Micro*, vol. 38, no. 1, pp. 82–99, Jan. 2018.

[4] M. R. Azghadi *et al.*, "Hardware implementation of deep network accelerators towards healthcare and biomedical applications," *IEEE Trans. Biomed. Circuits Syst.*, vol. 14, no. 6, pp. 1138–1159, Dec. 2020.

[5] S. Baek, J. K. Eshraghian, W. Thio, Y. Sandamirskaya, H. H. C. Iu, and W. D. Lu, "A real-time retinomorphic simulator using a conductance-based discrete neuronal network," in *Proc. 2nd IEEE Int. Conf. Artif. Intell. Circuits Syst. (AICAS)*, Aug. 2020, pp. 79–83.

[6] C. Arrow, H. Wu, S. Baek, H. H. C. Iu, K. Nazarpour, and J. K. Eshraghian, "Prosthesis control using spike rate coding in the retina photoreceptor cells," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2021, pp. 1–5.

[7] A. L. Hodgkin and A. F. Huxley, "A quantitative description of membrane current and its application to conduction and excitation in nerve," *J. Physiol.*, vol. 117, no. 4, pp. 500–544, 1952.

[8] L. Chua, V. Sbitnev, and H. Kim, "Hodgkin–Huxley axon is made of memristors," *Int. J. Bifurcation Chaos*, vol. 22, no. 3, Mar. 2012, Art. no. 1230011.

[9] L. O. Chua, "Memristor—The missing circuit element," *IEEE Trans. Circuit Theory*, vol. CT-18, no. 5, pp. 507–519, Sep. 1971.

[10] L. O. Chua and S. M. Kang, "Memristive devices and systems," *Proc. IEEE*, vol. 64, no. 2, pp. 209–223, Feb. 1976.

[11] D. B. Strukov, G. S. Snider, D. R. Stewart, and R. S. Williams, "The missing memristor found," *Nature*, vol. 453, no. 7191, pp. 80–83, May 2008.

[12] G. W. Burr *et al.*, "Neuromorphic computing using non-volatile memory," *Adv. Phys. X*, vol. 2, no. 1, pp. 89–124, 2017.

[13] R. Tetzlaff, *Memristors and Memristive Systems*. New York, NY, USA: Springer, 2013.

[14] J. K. Eshraghian *et al.*, "Neuromorphic vision hybrid RRAM-CMOS architecture," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 26, no. 12, pp. 2816–2829, Dec. 2018.

[15] R. Waser and M. Aono, "Nanoionics-based resistive switching memories," *Nanosci. Technol., Collection Rev. Nature J.*, pp. 158–165, Nov. 2010.

[16] X.-Y. Wang *et al.*, "High-density memristor-CMOS ternary logic family," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 68, no. 1, pp. 264–274, Jan. 2021.

[17] A. Ascoli, R. Tetzlaff, S.-M. Kang, and L. O. Chua, "Theoretical foundations of memristor cellular nonlinear networks: A DRM_2-based method to design memcomputers with dynamic memristors," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 67, no. 8, pp. 2753–2766, Aug. 2020.

[18] X. Wang, Z. Wu, P. Zhou, H. H. C. Iu, J. K. Eshraghian, and S. M. Kang, "FPGA synthesis of ternary memristor-CMOS decoders," 2021, *arXiv:2104.10297*.

[19] SM Corporation. (2020). *eFlash*. [Online]. Available: https://www.tsmc.com/english/dedicatedFoundry/technology/eflash.htm

[20] CMP. (2018). *Mad200 Memory Advance Demonstrator 200 mm*. [Online]. Available: https://mycmp.fr/datasheet/mad200-memory-advanced-demonstrator-200mm

[21] H.-S. P. Wong *et al.*, "Metal–oxide RRAM," *Proc. IEEE*, vol. 100, no. 6, pp. 1951–1970, Jun. 2012.

[22] J. K. Eshraghian, K. Cho, and S. M. Kang, "A 3-D reconfigurable RRAM crossbar inference engine," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, May 2021, pp. 1–5.

[23] S. H. Jo, T. Chang, I. Ebong, B. B. Bhadviya, P. Mazumder, and W. Lu, "Nanoscale memristor device as synapse in neuromorphic systems," *Nano Lett.*, vol. 10, no. 4, pp. 1297–1301, 2010.

[24] X. Zhu, C. Du, Y. Jeong, and W. D. Lu, "Emulation of synaptic metaplasticity in memristors," *Nanoscale*, vol. 9, no. 1, pp. 45–51, 2017.

[25] M. Rahimi Azghadi *et al.*, "Complementary metal-oxide semiconductor and memristive hardware for neuromorphic computing," *Adv. Intell. Syst.*, vol. 2, no. 5, Mar. 2020, Art. no. 1900189.

[26] A. Ascoli, A. S. Demirkol, R. Tetzlaff, S. Slesazeck, T. Mikolajick, and L. O. Chua, "On local activity and edge of chaos in a NaMLab memristor," *Frontiers Neurosci.*, vol. 15, p. 233, Apr. 2021.

[27] C. Lin *et al.*, "Adaptive synaptic memory via lithium ion modulation in RRAM devices," *Small*, vol. 16, no. 42, Oct. 2020, Art. no. 2003964.

[28] S. Kim, C. Du, P. Sheridan, W. Ma, S. H. Choi, and W. D. Lu, "Experimental demonstration of a second-order memristor and its ability to biorealistically implement synaptic plasticity," *ACS Nano*, vol. 15, no. 3, pp. 2203–2211, Feb. 2015.

[29] S. Gaba, P. Sheridan, J. Zhou, S. Choi, and W. Lu, "Stochastic memristive devices for computing and neuromorphic applications," *Nanoscale*, vol. 5, no. 13, pp. 5872–5878, 2013.

[30] C. Lammie, J. K. Eshraghian, W. D. Lu, and M. R. Azghadi, "Memristive stochastic computing for deep learning parameter optimization," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 68, no. 5, pp. 1650–1654, May 2021.

[31] Y. Yang, N. D. Truong, J. K. Eshraghian, A. Nikpour, and O. Kavehei, "Adaptive, unlabeled and real-time approximate-learning platform (AURA) for personalized epileptic seizure forecasting," *medRxiv 2021.09.30.21264287*, Nov. 2021.

[32] L. Lapicque, "Recherches quantitatives sur l'excitation electrique des nerfs traitee comme une polarization," *J. Physiol. Pathol.*, vol. 9, pp. 620–635, 1907.

[33] D. Noble, "A modification of the Hodgkin–Huxley equations applicable to Purkinje fibre action and pacemaker potentials," *J. Physiol.*, vol. 160, no. 2, pp. 317–352, Feb. 1962.

[34] D. Tal and E. L. Schwartz, "Computing with the leaky integrate-and-fire neuron: Logarithmic computation and multiplication," *Neural Comput.*, vol. 9, no. 2, pp. 305–318, Feb. 1997.

[35] C. Teeter *et al.*, "Generalized leaky integrate-and-fire models classify multiple neuron types," *Nature Commun.*, vol. 9, no. 1, pp. 1–15, Dec. 2018.

[36] R. Stein and A. L. Hodgkin, "The frequency of nerve action potentials generated by applied currents," *Proc. Roy. Soc. London B, Biol. Sci.*, vol. 167, no. 1006, pp. 64–86, 1967.

[37] J. K. Eshraghian *et al.*, "Training spiking neural networks using lessons from deep learning," 2021, *arXiv:2109.12894*.

[38] B. Choi *et al.*, "Resistive switching mechanism of TiO_2 thin films grown by atomic-layer deposition," *J. Appl. Phys.*, vol. 98, no. 3, 2005, Art. no. 033715.

[39] H.-S. P. Wong *et al.*, "Phase change memory," *Proc. IEEE*, vol. 98, no. 12, pp. 2201–2227, Dec. 2010.

[40] Y. Huai, "Spin-transfer torque MRAM (STT-MRAM): Challenges and prospects," *AAPPS Bull.*, vol. 18, no. 6, pp. 33–40, 2008.

[41] C. Li *et al.*, "Analogue signal and image processing with large memristor crossbars," *Nature Electron.*, vol. 1, no. 1, pp. 52–59, 2018.

[42] T. Serrano-Gotarredona, T. Masquelier, T. Prodromakis, G. Indiveri, and B. Linares-Barranco, "STDP and STDP variations with memristors for spiking neuromorphic learning systems," *Frontiers Neurosci.*, vol. 7, p. 2, Feb. 2013.

[43] J. K. Eshraghian, S.-M. Kang, S. Baek, G. Orchard, H. H.-C. Iu, and W. Lei, "Analog weights in ReRAM DNN accelerators," in *Proc. IEEE Int. Conf. Artif. Intell. Circuits Syst. (AICAS)*, Mar. 2019, pp. 267–271.

[44] X. Zhang *et al.*, "An artificial neuron based on a threshold switching memristor," *IEEE Electron Device Lett.*, vol. 39, no. 2, pp. 308–311, Feb. 2018.

[45] X. Zhu, Q. Wang, and W. D. Lu, "Memristor networks for real-time neural activity analysis," *Nature Commun.*, vol. 11, no. 1, pp. 1–9, Dec. 2020.

[46] R. Wang *et al.*, "Recent advances of volatile memristors: Devices, mechanisms, and applications," *Adv. Intell. Syst.*, vol. 2, no. 9, Sep. 2020, Art. no. 2000055.

[47] M. D. Pickett, G. Medeiros-Ribeiro, and R. S. Williams, "A scalable neuristor built with Mott memristors," *Nature Mater.*, vol. 12, no. 2, pp. 114–117, Dec. 2012.

[48] Q. Duan *et al.*, "Spiking neurons with spatiotemporal dynamics and gain modulation for monolithically integrated memristive neural networks," *Nature Commun.*, vol. 11, no. 1, pp. 1–13, Dec. 2020.

[49] A. Ascoli, S. Slesazeck, H. Mähne, R. Tetzlaff, and T. Mikolajick, "Nonlinear dynamics of a locally-active memristor," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 62, no. 4, pp. 1165–1174, Apr. 2015.

[50] E. J. Fuller *et al.*, "Parallel programming of an ionic floating-gate memory array for scalable neuromorphic computing," *Science*, vol. 364, no. 6440, pp. 570–574, May 2019.

[51] E. R. Kandel, J. H. Schwartz, T. M. Jessell, S. Siegelbaum, A. J. Hudspeth, and S. Mack, *Principles of Neural Science*, vol. 4. New York, NY, USA: McGraw-Hill, 2000.

[52] C. S. Thakur *et al.*, "Large-scale neuromorphic spiking array processors: A quest to mimic the brain," *Frontiers Neurosci.*, vol. 12, p. 891, Dec. 2018.

[53] M. J. Rozenberg, O. Schneegans, and P. Stoliar, "An ultra-compact leaky-integrate-and-fire model for building spiking neural networks," *Sci. Rep.*, vol. 9, no. 1, pp. 1–7, Dec. 2019.

[54] S. M. Sherman, R. W. Guillery, and G. M. Shepherd, *Synaptic Organization of the Brain*. Oxford, U.K.: Oxford Univ. Press, 2004.

[55] K. Wang *et al.*, "Threshold switching memristor-based stochastic neurons for probabilistic computing," *Mater. Horizons*, vol. 8, no. 2, pp. 619–629, 2021.

[56] J. Lin *et al.*, "Low-voltage artificial neuron using feedback engineered insulator-to-metal-transition devices," in *IEDM Tech. Dig.*, Dec. 2016, pp. 5–34.

[57] P. Stoliar *et al.*, "A leaky-integrate-and-fire neuron analog realized with a Mott insulator," *Adv. Funct. Mater.*, vol. 27, no. 11, 2017, Art. no. 1604740.

[58] Z. Wang *et al.*, "Fully memristive neural networks for pattern classification with unsupervised learning," *Nature Electron.*, vol. 1, pp. 137–145, Feb. 2018.

[59] Z. Wang *et al.*, "Capacitive neural network with neuro-transistors," *Nature Commun.*, vol. 9, no. 1, pp. 1–10, Dec. 2018.

[60] R. J. Baker, "Resistive memory element sensing using averaging," U.S. Patent 6 504 750 B1, Jul. 1, 2003.

[61] R. Toro *et al.*, "Brain size and folding of the human cerebral cortex," *Cerebral Cortex*, vol. 18, no. 10, pp. 2352–2357, Oct. 2008.

[62] S. M. Kang, R. H. Krambeck, H. F. S. Law, and A. D. Lopez, "Gate matrix layout of random control logic in a 32-bit CMOS CPU chip adaptable to evolving logic design," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. CAD-2, no. 1, pp. 18–29, Jan. 1983.

[63] Q. Wang, X. Wang, S. H. Lee, F.-H. Meng, and W. D. Lu, "A deep neural network accelerator based on tiled RRAM architecture," in *IEDM Tech. Dig.*, Dec. 2019, pp. 4–14.

[64] T. Delbruck, "Neuromorphic AI tutorial session," in *Proc. IEEE Int. Conf. Artif. Intell. Circuits Syst.*, Hsinchu, Taiwan, Mar. 2019.

[65] L. A. Hart, *How The Brain Works*. New York, NY, USA: Basic Books, 1975.

[66] Harvard Health Publishing. (2018). *Calories Burned in 30 Minutes for People of Three Different Weights*. [Online]. Available: https://www.health.harvard.edu/newsweek/Calories-burned-in-30-minutes-of-leisure-and-routine-activities.htm

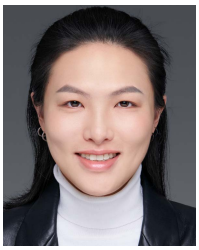
[67] B. P. Bean, "The action potential in mammalian central neurons," *Nature Rev. Neurosci.*, vol. 8, no. 6, pp. 451–465, 2007.

[68] B. A. Olshausen and D. J. Field, *What is the Other 85 Percent of V1 Doing*, vol. 23, L. van Hemmen and T. Sejnowski, Eds. Oxford, U.K.: Oxford Univ. Press, 2006, pp. 182–211.

Sung Mo (Steve) Kang (Life Fellow, IEEE) received the B.S. degree *(summa cum laude)* from Fairleigh Dickinson University, Teaneck, NJ, USA, the M.S. degree from the State University of New York, Buffalo, and the Ph.D. degree from UC Berkeley. He was the 15th President of the Korea Advanced Institute of Science and Technology (KAIST), the Second Chancellor of the University of California, Merced, the Dean of engineering with the University of California, Santa Cruz, and the Department Head of electrical and computer engineering at the University of Illinois at Urbana-Champaign. He is currently a Distinguished Professor with the Jack Baskin School of Engineering, UC Santa Cruz. He holds 16 U.S. patents. He has authored ten books and published over 500 journals and conference papers. His current research interests include memristors and memristive systems, neuromorphic computing, low-power VLSI design, and compact modeling for computer-aided design. He is a fellow of ACM and AAAS.

Donguk Choi received the bachelor's degree in physics and the master's degree in nuclear engineering from Seoul National University in 1990 and 1994, respectively. He is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering, University of California, Santa Cruz. From 1994 to 2018, he worked at Samsung Electronics as a Device Engineer. His research is focused on neuromorphic computing, especially memristive spiking neural networks.

Jason K. Eshraghian (Member, IEEE) received the Bachelor of Engineering (electrical and electronic) and Bachelor of Laws degrees from The University of Western Australia, WA, Australia, in 2017, and the Ph.D. degree from The University of Western Australia in 2019. He is currently a Post-Doctoral Researcher at the Department of Electrical Engineering and Computer Science, University of Michigan, Ann Arbor, and a Forrest Research Fellow with the Department of Computer Science and Software Engineering and the School of Computer Science and Medicine, The University of Western Australia. He is the Developer of *snnTorch*. His current research interests include neuromorphic computing, resistive random access memory (RRAM) circuits, and spiking neural networks. He serves as the Secretary-Elect for the IEEE Neural Systems and Applications Committee. He was awarded the 2019 IEEE Very Large Scale Integration Systems Best Paper Award, the Best Paper Award at the 2019 IEEE Artificial Intelligence Circuits and Systems Conference, and the Best Live Demonstration Award at the 2020 IEEE International Conference on Electronics, Circuits and Systems. He was a recipient of the Fulbright Fellowship (Australian–American Fulbright Commission), the Forrest Research Fellowship (Forrest Research Foundation), and the Endeavour Fellowship (Australian Government).



Peng Zhou (Member, IEEE) received the Bachelor of Engineering degree from the Huazhong University of Science and Technology in 2016 and the master's degree from the University of California, Santa Cruz, where she is currently pursuing the Ph.D. degree with the Department of Electrical and Computer Engineering. Her research is focused on neuromorphic computing, especially spiking neural networks and their hardware implementation using memristors.

Jieun Kim received the B.S. degree from the Department of Electronic and Electrical Engineering, Sungkyunkwan University, Suwon, South Korea, in 2019, where she is currently pursuing the M.S. degree with the Department of Electrical and Computer Engineering. Her research is focused on bioinspired-learning algorithms and neuromorphic computing, especially the design and implementation of spiking neural networks.

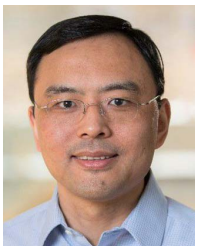
Bai-Sun Kong (Member, IEEE) received the B.S. degree in electronics engineering from Yonsei University, Seoul, South Korea, in 1990, and the M.S. and Ph.D. degrees in electrical engineering from the Korea Advanced Institute of Science and Technology (KAIST), Daejon, South Korea, in 1992 and 1996, respectively. Since 1996, he has been a Senior Design Engineer with LG Semicon Company (currently SK Hynix Corporation), Seoul, where he was working on the design of high-density and high-bandwidth DRAMs. In 2000, he joined the Faculty of Korea Aerospace University, Goyang, South Korea, as an Assistant Professor with the School of Electronics Telecommunication and Computer Engineering. In 2005, he moved to Sungkyunkwan University, Suwon, South Korea, where he is currently a Professor with the College of Information and Communication Engineering. From 2018 to 2019, he was with the Center for Nanotechnology, NASA Ames Research Center, CA, USA, and the Nanoelectronic Integrated Systems Laboratory, University of California at Santa Cruz, CA, USA, where he has been doing collaborative research on neuromorphic integrated circuit design. His research interests include high-speed low-power microprocessor and (or) memory circuit design, high-speed wireline transceiver design, fast-transient high-efficiency DC-DC converter design, and IC design for neuro-inspired applications.

Xiaojian Zhu received the B.S. degree in physics from Soochow University, China, in 2009, and the Ph.D. degree in material science from the University of Chinese Academy of Sciences, China, in 2014. From 2015 to 2020, he worked as a Post-Doctoral Research Fellow with the Electrical Engineering and Computer Science Department, University of Michigan. He is currently a Full Professor at the Ningbo Institute of Materials Technology and Engineering and the Deputy Director of the Key Laboratory of Magnetic Materials and Devices, Chinese Academy of Sciences. His research interests include nanoionic materials and devices for neuromorphic computing.

Ahmet Samil Demirkol received the Ph.D. degree in electronics engineering from Istanbul Technical University in 2014. Since 2019, he has been a Research Associate with the Chair of Fundamentals of Electrical Engineering, TU Dresden. His current research interests cover modeling of memristors, analysis and design of memristive systems, cellular nonlinear networks, and neuromorphic circuit design, while he has a strong background in analog circuit design, active network synthesis, and nonlinear dynamics and chaos.

Alon Ascoli (Member, IEEE) received the Ph.D. degree in electronic engineering from University College Dublin in 2006. Since 2012, he has been a Lecturer at the Faculty of Electrical and Computer Engineering, Technische Universität Dresden. He develops system-theoretic methods for the analysis and design of bio-inspired memristive circuits. He was honoured with the Best Paper Awards from IJCTA in 2007 and MOCAST in 2020. In April 2017, he was conferred the habilitation title as an Associate Professor in electrical circuit theory from the Italian Ministry of Education. He is currently the President of the IEEE Cellular Nonlinear Networks and Memristive Array Computing (CNN-MAC) Technical Committee.

Ronald Tetzlaff (Senior Member, IEEE) is currently the Chief Officer for technology transfer and internationalization at Technische Universität Dresden, Dresden, Germany, where he also holds a Full Professorship in fundamentals of electrical engineering. His scientific interests include problems in the theory of signals and systems, medical signal processing, stochastic processes, system modeling, system identification, machine learning, mem-elements, memristive systems, volterra systems, and cellular nonlinear networks.



Wei D. Lu (Fellow, IEEE) received the B.S. degree in physics from Tsinghua University, Beijing, China, in 1996, and the Ph.D. degree in physics from Rice University, Houston, TX, USA, in 2003. From 2003 to 2005, he was a Post-Doctoral Research Fellow at Harvard University, Cambridge, MA, USA. He joined the Faculty of the University of Michigan in 2005. He is currently a Professor with the Electrical Engineering and Computer Science Department, University of Michigan. His research interests include resistive-random access memory (RRAM), memristor-based logic circuits, neuromorphic computing systems, aggressively scaled transistor devices, and electrical transport in low-dimensional systems. He was a recipient of the NSF CAREER Award.

Leon O. Chua (Life Fellow, IEEE) was a Foreign Member of the European Academy of Sciences (Academia Europaea) in 1997 and the Hungarian Academy of Sciences in 2007. He is widely known for his invention of the Memristor. When not immersed in science, he relaxes by searching for Wagner's leitmotifs, musing over Kandinsky's chaos, and contemplating Wittgenstein's inner thoughts. His research has been recognized through 17 honorary doctorates from major universities in Europe and Japan and holds seven U.S. patents. He was elected as a Confrerie des Chevaliers du Tastevin in 2000. He was conferred numerous prestigious awards, including the First Kirchhoff Award, the Guggenheim Fellow, the 2019 EDS Celebrated Member Prize—The highest recognition of the IEEE Electron Devices Society, and the 2020 Julius Springer Prize in Applied Physics.