

PAPER

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9, 14799**10 MA cm⁻² current density in nanoscale
conductive bridge threshold switching selector
via densely localized cation sources†**Qi Lin,^a Jinlong Feng,^a Junhui Yuan,^a Long Liu,^a Jason K. Eshraghian,^b
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Conductive bridge threshold switching (CBTS) selector is a selector candidate for large-scale 3D crosspoint memory. In spite of its high selectivity, the generally low current density (J_{ON}) of $<0.5 \text{ MA cm}^{-2}$ is not practical for driving the memory elements. In particular, J_{ON} is the determining factor for the 3D PCM application owing to the greatly increased RESET current density in PCM cells as the size scales down. The low J_{ON} of CBTS selectors originates from the reduced number of conductive filament (CF) as the device scales down and the CF overgrowth induced long lifetime at a large current. Here, a strategy of inserting the super-ionic cation layer to form densely distributed Cu-rich cation sources is proposed to modulate the quantity and size of CFs. Multiple CFs grow from the cation sources to conduct current in parallel and CF overgrowth is prevented by local cation injection. The fabricated Pt/Cu₂S/GeSe/Pt devices achieve a record 10 MA cm^{-2} J_{ON} and $5 \text{ mA } I_{\text{drive}}$, realizing a ten-fold increase in the J_{ON} in CBTS selectors. Moreover, the selectivity is the highest at 10^{10} , and the switching slope is $<0.18 \text{ mV dec}^{-1}$. The high-resolution transmission electron microscopy (HRTEM) image reveals multiple single-crystal nanochannels distributed in the Cu₂S layer with a diameter of $\sim 20 \text{ nm}$ and a distance of $15\text{--}20 \text{ nm}$, suggesting dense CF paths of small size. This method is practical for fabricating a scalable selector owing to the dense CF paths. The breakthrough in J_{ON} will greatly promote the practical use of CBTS selectors in 3D crosspoint memory.

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rsc.li/materials-c**Introduction**

The main factor that determines a memory system's cost is the integration density of the components, which decides the yield of each single wafer. 3D crosspoint memory currently provides the highest density solution for storage class memory (SCM) and neuromorphic computing.^{1,2} A two-terminal selector is an essential building block of 3D crosspoint memory to address the “sneak current” issue, *i.e.*, the undesired current paths flowing through the half-biased memory cells. Threshold switching (TS) selectors, categorized into Ovonic TS (OTS) selectors, Mott TS selectors, and conductive bridge TS (CBTS) selectors, are commercially preferable candidates owing to the high selectivity to improve the read/write margin for large-scale array implementation.^{1,3}

OTS selectors, based on the electronic conduction of trapped states in amorphous chalcogenides, are popular owing to their large

J_{ON} and fast switching.^{4,5} However, it suffers from high leakage and complex material engineering including the toxic arsenic element.^{4,6} The Mott TS selector utilizes electrically strong coupled materials such as VO₂ or NbO₂, which shows ultrafast switching speed and theoretically unlimited endurance due to slight atomic displacement on phase transition.^{7,8} Unfortunately, the off-state semiconductor phase is highly conducting, resulting in the poor selectivity of <100 and high leakage.⁸ Besides, the process temperature of VO₂ deposition is $>500 \text{ }^{\circ}\text{C}$, which is not stackable. In this sense, the CBTS selector, which switches by cation migration-induced CF connection/disconnection, stands out for the potential of very large-scale integration owing to the high selectivity of $>10^7$.^{9,10} Moreover, the material composition is simple and the fabrication temperature is not destructive to the 3D process. However, the driving current (I_{drive}) of CBTS selectors drops greatly on scaling down, resulting in a poor J_{ON} of $<0.5 \text{ MA cm}^{-2}$.^{10,11} In order to integrate with nanoscale PCM in $4F^2$ crosspoint array, a J_{ON} of 8 MA cm^{-2} is necessary because the PCM reset current density greatly increases for smaller critical dimension.^{12,13} Besides, the state-of-the-art OTS selectors capable of providing 8 MA cm^{-2} J_{ON} demonstrated the integration with PCM.^{4,14} Therefore, it is urgently needed to enhance the J_{ON} of well-rounded CBTS selectors to match the integration.

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The low J_{ON} in CBTS selectors is attributed to two main factors: (1) the number of CFs decreases on scaling.^{15,16} (2) The CFs of large current capability have long lifetime, causing undesired non-volatile switching.^{15,17,18} To improve the J_{ON} , a possible solution is to increase the number of CFs in the nanoscale devices while confining the CF size to prevent overgrowth. Zhao X. *et al.* inserted impermeable graphene with discrete defects between the electrode and the switching layer to modulate the CF size and quantity, which realized ~ 1 mA I_{drive} in the $4\ \mu\text{m}$ device size, breaking the current-retention dilemma of CBTS selectors.¹⁵ The J_{ON} of the graphene devices is $0.01\ \text{MA cm}^{-2}$ owing to the large lateral size and demonstration of the nanoscale devices is lacking. Considering that the observed CF paths in the graphene devices are at a distance from 40 to 150 nm, a potential issue for nanoscale application is that higher-density CFs require higher Si^+ irradiation fluence, which could enlarge the defect size and result in memory switching. The practical implementation requires a scalable and high J_{ON} scheme.

In this article, a super-ionic Cu_2S cation layer capped on the GeSe switching medium is proposed to create multiple Cu-rich cation sources with a diameter of ~ 20 nm and an interval of merely 15–20 nm, guaranteeing a large number of CFs even in nanoscale devices. The localized cation injection of these sources also controls the CF size to prevent the overgrowth. The fabricated Pt/ Cu_2S /GeSe/Pt devices realize a record J_{ON} of $10\ \text{MA cm}^{-2}$ in 250 nm lateral size, making it possible to integrate with the PCM in 4F^2 crosspoint architecture.¹² The selectivity reaches 10^{10} , effectively preventing the leakage for high-density integration. The switching slope is the sharpest at

$< 0.18\ \text{mV dec}^{-1}$. The simple sputtering fabrication without any high-temperature process is industrially practical and 3D stackable. The method is applicable to other superionic materials of wide choices including Ag_2Te , Ag_2Se , Ag_2S , Cu_2Se , and Cu_2Te .^{19,20} The transmission electron microscopy (TEM) image reveals many single-crystal nanochannels in the Cu_2S ionic layer as the traces of local cation sources. These nanochannels are closely distributed with diameters of ~ 20 nm and spacing of 15–20 nm, indicating a large CF density and thin CF size. The process of creating cation sources is verified by the observed twinning crystal and Cu-deficient djurite phase after field-assisted cation migration. The breakthrough of the current density wall will accelerate the commercial progress of the CBTS selectors toward 3D crosspoint memory applications.

Results and discussion

High J_{ON} and large selectivity in scaled nano devices

Prototypes of 3D crosspoint PCM were released by Intel/Micron and SK-Hynix companies, as shown in the schematic of Fig. 1(a).^{2,21} Each deck integrates a two-terminal memory (R) and selector (S). A scalable selector of high J_{ON} is essential for memory integration and dense storage. Here, we proposed to introduce super-ionic Cu_2S cation layer to create many Cu-rich cation sources to increase the quantity and confine the size of CFs to realize a scalable selector with large J_{ON} , as illustrated in Fig. 1(b). Accordingly, the Pt/ Cu_2S /GeSe/Pt devices were fabricated and verified by the TEM observation on the cross-section. The devices in a 250 nm diameter *via*-hole structure separated

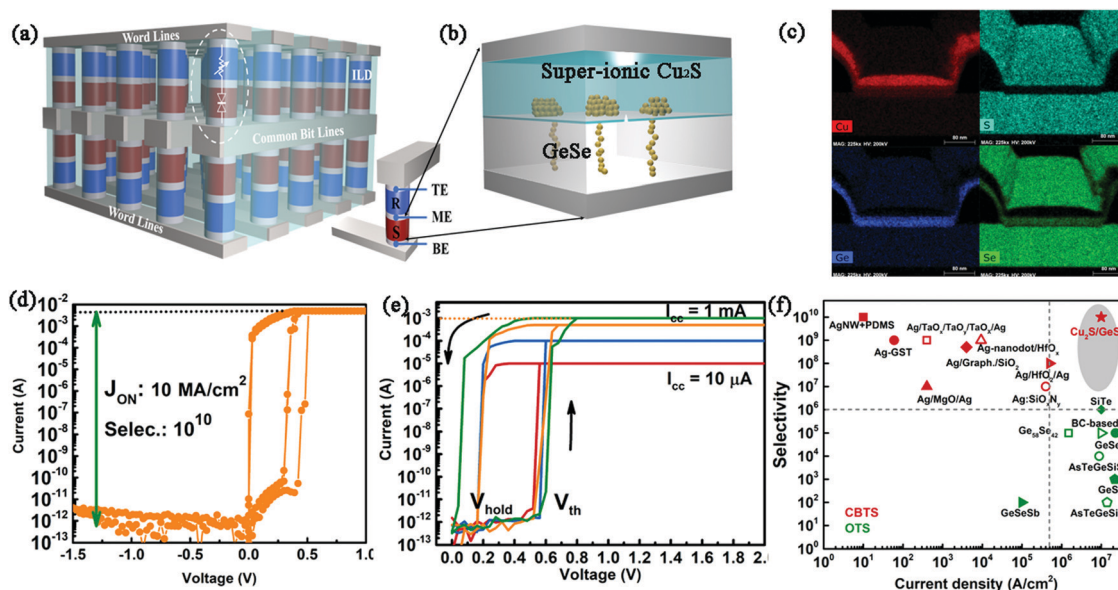


Fig. 1 (a) Two-deck 3D crosspoint memory architecture integrating one selector and one memory element in each cell. (b) Schematic of localized Cu-rich cation sources that encourage multiple Cu CFs growth in the proposed Pt/ Cu_2S /GeSe/Pt selector. (c) EDS element mapping of the as-prepared Pt/ Cu_2S /GeSe/Pt devices in a 250 nm diameter *via*-hole. (d) Switchable IV curves of the Pt/ Cu_2S /GeSe/Pt device show 5 mA driving current and 10^{10} selectivity, with a record J_{ON} of $10\ \text{MA cm}^{-2}$. (e) The selector can work at a lower compliance current. (f) The selectivity *versus* current density benchmark of CBTS selectors in red and OTS selectors in green. The Cu_2S /GeSe-based selector (red star) in this paper reaches higher selectivity and has comparable current density to OTS selectors.

by SiO₂ insulating dielectrics with the shared bottom electrode, as shown in the TEM image of Fig. S1 (ESI†). Energy dispersive spectrometer (EDS) element mappings in Fig. 1(c) indicate the well-deposited Cu₂S cation layer and the GeSe switching layer. The Cu atomic concentration in Cu₂S is 63% by X-ray photoelectron spectroscopy (XPS) measurements. The X-ray diffraction (XRD) in Fig. S2 (ESI†) shows crystallized monoclinic lattice in the as-deposited Cu₂S film.²² The only stray peak near 50 degrees stems from the djurleite phase (Cu_xS, 1.93 < *x* < 1.97).²³ The GeSe switching medium is the Se-rich Ge₄Se₆, as confirmed by EDS. Later, the amorphous GeSe film was heated from 50 to 550 °C and detected by *in situ* XRD in real time, showing no crystallizing degradation, which is back-end-of-line (BEOL) compatible (Fig. S3, ESI†).

The *I*-*V* properties of the Pt/Cu₂S/GeSe/Pt devices was then characterized by DC sweeping, as indicated in Fig. 1(d). The selector can provide 5 mA operating current for nanoscale memory elements. The *J*_{ON} is 10 MA cm⁻², which enables the selector to drive nanoscale PCM in 4F² footprint array. Meanwhile, the selectivity is 10¹⁰, among the highest ones in CBTS selectors, promising large-scale integration. Fig. 1(e) shows the reliable switching of the Pt/Cu₂S/GeSe/Pt selector under a lower working current of 10 μA, 100 μA, 500 μA, and 1 mA. The benchmark of selectivity *versus* the *J*_{ON} of the state-of-the-art CBTS selectors and commercially preferred OTS selectors is shown in Fig. 1(f).^{4,6,11,15–17,24–33} While the selectivity of the CBTS selectors is above 10⁶, the current density is generally lower than 0.5 MA cm⁻². In contrast, the OTS selectors achieved a *J*_{ON} of ~8 MA cm⁻², even integrated with PCM in some cases, yet equipped with a selectivity below 10⁶. The Cu₂S/GeSe-based selector in this work realizes 10 MA cm⁻² *J*_{ON} while presenting

10¹⁰ selectivity at the same time, throwing light on the commercialization of the CBTS selectors for 4F² PCM memory.

Further, device reliability on cycling, switching speed, leakage block, and uniformity were explored. Fig. 2(a) shows repeated DC switching of the Cu₂S/GeSe-based selector under a large *I*_{drive} of 1 mA for 100 cycles. The selectivity is 10¹⁰ with a leakage of <1 pA, promising low-power and large-size array scheme. By the slow sweep of 0.8 mV per step, the selector shows the sharpest switching slope (SS) of <0.18 mV dec⁻¹ in Fig. 2(b). Due to this, the high *I*_{drive} greatly undermines the selector performances, and the DC cycling of hundred times with 1 mA current has been rarely reported.^{11,15,16} The reliable cycling at a large current in this work is attributed to several tiny CFs, which conduct current in parallel and meanwhile remain volatile due to the short CF lifetime.¹⁷ The fast switching speed also supports the tiny size and large number of CFs. The selector builds the CF connection within 150 ns while relaxing back in no longer than 250 ns, as shown in the up panel of Fig. 2(c). A sequence of 2 V/1 μs pulses was next applied and confirmed 150/250 ns on/off speed (the lower panel of Fig. 2(c)). On the endurance test, to ensure that the devices switch at each pulse cycle, we imposed 4 V/5 μs pulse sequences with 5 μs interval on the devices. The switching is reliable after 10⁶ writing times, as shown in Fig. 2(d). Here, a 1 MΩ series resistor is connected to prevent the damage of the large overshoot current. Next, 100 mV bias is applied on the selector for 20 ks to imitate the leakage disturbance. The current remains below 1 pA during the entire DC stress test. The device uniformity was next investigated. From device to device, the statistical histogram in Fig. S4 (ESI†) shows the threshold voltage (*V*_{th}) distribution spanning from 0.4 V to 0.6 V with a

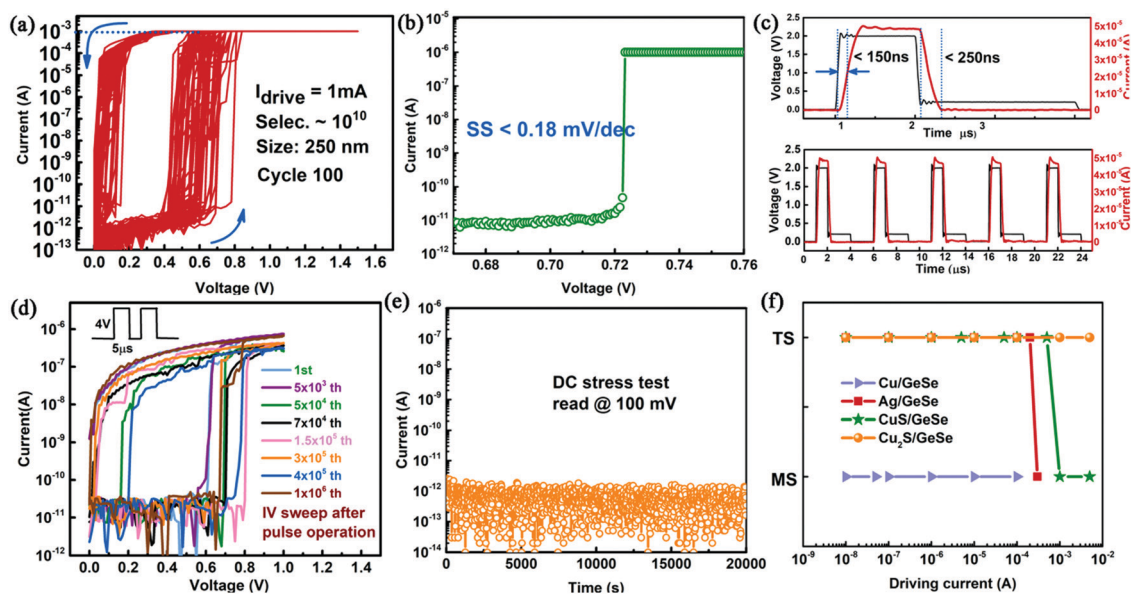


Fig. 2 (a) The DC sweep of 100 switching cycles under a *I*_{drive} of 1 mA. (b) Sharp switching slope of <0.18 mV dec⁻¹. (c) On/off switching speed of 150/250 ns. (d) Pulse endurance of >10⁶ at 4 V/5 μs writing pulse condition. (e) DC stress test at 0.1 V for 20 ks. (f) The TS and MS behavior of Cu/GeSe, Ag/GeSe, CuS/GeSe, and Cu₂S/GeSe-based selectors at different currents.

mean value of 0.48 V. From cycle to cycle, the off-current is at about the fA level with negligible fluctuation (Fig. S5, ESI†). Besides, a 0.2 V operating window lies between the holding voltage (V_{hold}) and V_{th} during the cycling (Fig. S6, ESI†). There is no electroforming requiring a large electric field. The selectors could be reliably operated for 18 months after the fabrication, as in Fig. S7 (ESI†).

Cu/GeSe-, CuS/GeSe-, and Ag/GeSe-based selectors were fabricated as a comparison to highlight the effect of the local cation sources in the Cu_2S /GeSe devices. According to Fig. 2(f), the Cu/GeSe-based selector with unlimited copper injection shows memory switching (MS) at a compliance current (I_{CC}) as low as 10 nA. The reliable MS switching of the Cu/GeSe devices is shown in Fig. S8 (ESI†). When limiting copper by the alloy electrode, the CuS/GeSe-based selector can take an I_{drive} of 500 μA but becomes non-volatile at 1 mA, as shown in Fig. S9 (ESI†). The Cu_2S /GeSe-based selector with localized cation sources, however, remains TS above 5 mA I_{drive} . The Cu/GeSe-based selector facilitates fast CF overgrowth, resulting in MS.¹⁷ Replacing Cu with CuS increases the CF overgrowth resistance. However, the number of CFs cannot be effectively increased. We also replaced Cu with the fast species Ag, which is known for its high diffusion coefficient in dielectrics to facilitate CF diffusion. The result in Fig. S10 (ESI†) indicates the TS below 200 μA and MS at 300 μA . Above all, introducing multiple cation sources by Cu_2S , which confines the CF size and increases the number of CFs, is the most effective way to improve the I_{drive} .

The Cu_2S /GeSe-based selector also shows potential for high-density artificial synaptic array implementation for constructing neuromorphic systems. The device emulates synapse on short-term plasticity (STP) including paired-pulse facilitation (PPF) and paired-pulse depression (PPD) at different voltage pulse frequency.³⁴ As shown in Fig. S11 (ESI†), a train of pulses (spikes) swept at a frequency of 560 Hz induces a gradual increase in the current. Further modulating the pulse frequency to 200 Hz can lead to the depression of the current owing to the short-term memory.

Origin of high CF density by creating localized cation sources

To clarify the underlying physics behind the high- J_{ON} switching behavior, extensive high-resolution TEM (HRTEM) analysis was performed to visualize the nanostructure change of heavily

cycled devices. “Nanochannel” crystalline phases, which are believed to be localized cation sources, were observed in many locations inside the Cu_2S layer. As shown in Fig. 3(a), nanochannel crystals are densely distributed in the Cu_2S layer with small spacing, e.g., at spot 1, 2, and 3. Meanwhile, the GeSe layer is clear without any crystallization or clustering. The crystal structures of these nanochannels are further characterized in Fig. 3(b) and (c). The nanochannels at spots 1 and 2 show uniform hexagonal sulfur sublattice fringe of the (101) crystal planes with an interplanar spacing of $d = 0.305$ nm, indicating a high chalcocite (HC) phase.¹⁹ The crystal channel at spot 3 is a low chalcocite (LC) phase with a monoclinic lattice of the (630) planes with a d spacing of 0.197 nm.¹⁹ As a comparison, the crystallization of the areas surrounding the nanochannels indicates small grains of the LC phase in the (106) crystal planes or the HC phase at the (002) crystal planes, as shown in Fig. S12 (ESI†).

The nanochannels are characterized as single crystals instead of polycrystalline ones due to repeated heat-induced coarsening. Initially, the Cu_2S layer is deposited by fast sputtering at room temperature; thus, the grain size is small, as shown in Fig. S12 (ESI†). Annealing energy is required for these small grains to grow into the as-observed single-crystal nanochannels.^{35,36} These single-phase nanochannels were also reported in VO_2 Mott selectors as a result of the electroforming operation, which activates grain coarsening.^{35,36} In the proposed Pt/ Cu_2S /GeSe/Pt selector, thermal annealing from the connected CFs can provide the energy for grain coarsening, considering the high thermal effect of the Cu CFs. The repeated Joule heating from CFs at fixed positions result in the growth of small grains into large single-crystal nanochannels in these areas, suggesting that CFs form at the nanochannel locations. The distances between the large grains in Fig. 3 are in the range of 15–20 nm. The closely distributed nanochannels suggest significantly increased number of CFs. The diameter of ~ 20 nm could confine the CF size by limiting the cation injection area to prevent MS induced by CF overgrowth.¹⁸

The reason why we believe these nanochannels are cation sources is that the formation process of the cation sources leaves traces, which were observed by TEM, as shown in Fig. 4. Here, we first explain how the cation sources are formed in the designed selector based on the super-ionic cation layer. The Cu_2S cation layer can transform into the super-ionic HC phase

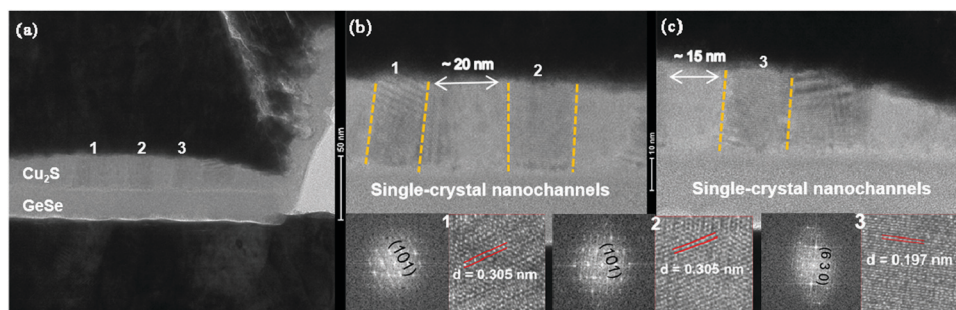


Fig. 3 Traces of cation sources and CFs revealed by densely distributed single-crystal nanochannels with diameters of ~ 20 nm and spacing in the range of 15–20 nm.

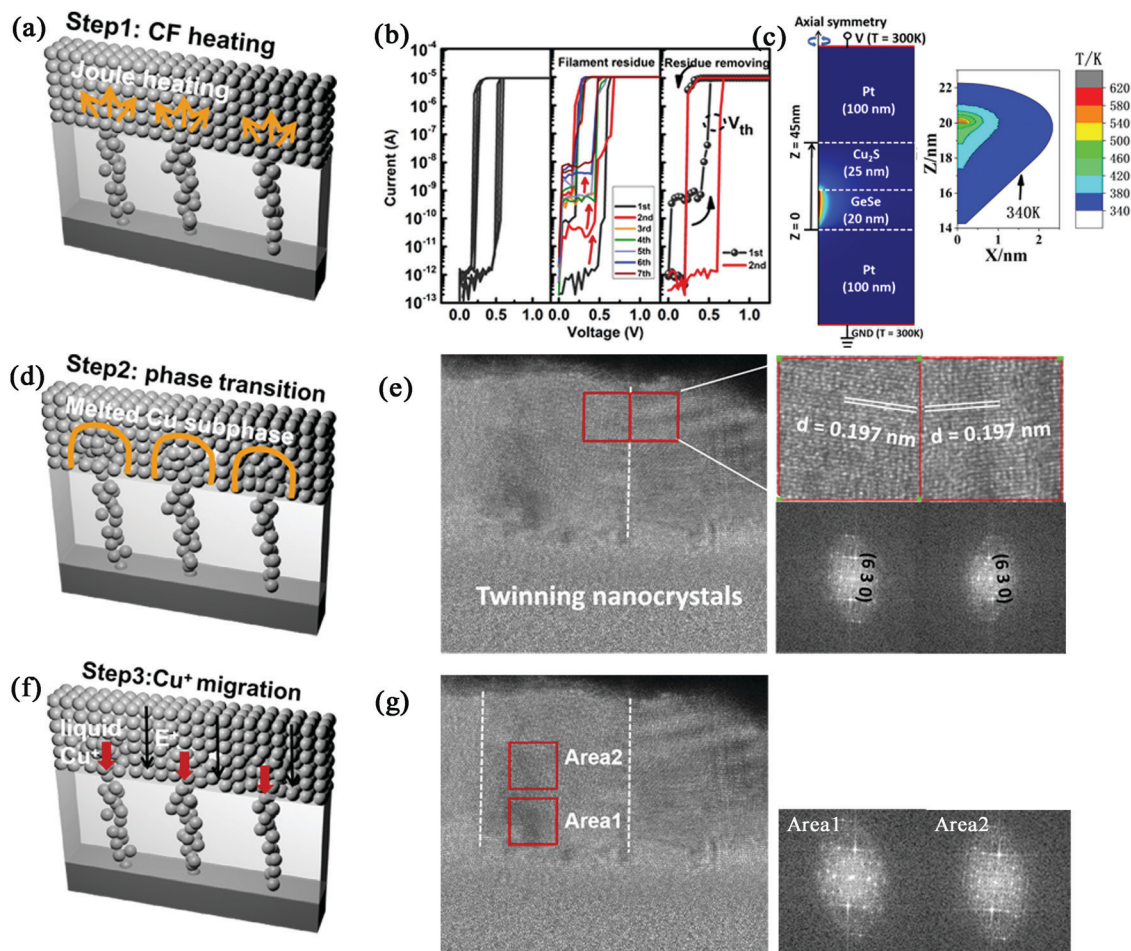


Fig. 4 Three processes for the generation of localized cation sources. (a) The schematic of CF Joule heating the local areas of Cu₂S to over 370 K. (b) Electrical annealing operations to repeatedly heat the local areas. (c) Thermal simulation of the electrical annealing operation, which elevates the temperature of the Cu₂S boundary to over 340 K within a certain range. (d) Schematic of the super-ionic Cu₂S phase with the melted Cu subphase in the heated areas by phase transformation. (e) Twinning nanocrystals as a result of phase transformation. (f) Schematic of field-assisted copper migration. (g) Cu-rich chalcocite phase in Area1 and Cu-poor djurleite phase in Area2 indicate copper migration along the electric field.

with a melted copper subphase at >370 K. This temperature condition could be created by the Joule heating of Cu CFs.³⁷ Combining these two effects, superionic phases with liquid Cu⁺ would be generated and migrate toward the heated locations along the electric field direction. Cu-rich cation sources were then formed by copper aggregation. The three essential processes of CF Joule heating, Cu₂S phase change, and Cu⁺ migration were supported by the evidences shown in Fig. 4.

The first process is the CF Joule heating effect, as shown in the schematic of Fig. 4(a). The IV curves of the selector before the stable operating state in Fig. 4(b) shows the electrical annealing process. The off-state current during electrical annealing is low at first and then gradually increases, followed by a sudden drop. The direct-tunneling fitting of the off-state current in Fig. S13 (ESI[†]) and the accordingly changed V_{th} in Fig. S14 (ESI[†]) suggests the CF residue remaining and its removal. The CFs are rebuilt on these residues to repeatedly heat the same areas, contributing to copper aggregation. We then simulated the thermal effect of the CFs during the

electrical annealing process, as shown in Fig. 4(c). The TE and BE are bound to be 300 K and the CF conductance is set to be consistent with the real case. The detailed parameters are listed in Table SI (ESI[†]). The temperature contour plot in Fig. 4(c) shows that 2 nm depth into the Cu₂S layer is heated over 340 K. Given that T_p is strongly size-dependent, which decreases to 337 ± 4 K for nanorods,³⁸ more than 2 nm depth of Cu₂S would be melted.

The second process is Cu₂S phase transformation from the solid LC phase to the superionic HC phase with melted Cu⁺ subphase, as described in Fig. 4(d). The transition is reversible, which recovers to the LC phase after cooling down; thus, the HC phase cannot be directly observed using TEM at room temperature. The HC phase shown in Fig. 3(c) is caused by the electron dose influence.³⁹ However, this leaves the twinning crystal as the traces of phase transition. Note that there are two monoclinic nanochannels of the (630) crystal planes growing into the twinning structure, as shown in Fig. 4(e). The symmetric lattice fringes' direction with the same d-spacing of

0.197 nm further confirms the twinning crystal. Normally, the atomic rearrangement on cooling down after reversible high-temperature phase transformation encourages the intergrowth of the twinning crystals, *i.e.*, the so-called transformation twins.^{40,41} In our case, the transformation twins are generated when the HC phase transits back to the LC phase at a temperature of <370 K. As a support, the tendency that small grains grow into nanochannels in Pt/Cu₂S/GeSe/Pt devices is consistent with the characteristics of the transformation twins that their shape is determined by the minimization of the interfacial energy.

The third process is that liquid Cu⁺ migrate along the electric field to accumulate near the boundary of Cu₂S/GeSe, as depicted in Fig. 4(f). Field-assisted copper migration could result in the transformation of the chalcocite (Cu₂S) phase to the djurleite (Cu_{1.93} to 1.97S) phase owing to the increased Cu vacancies.⁴² The FFT reflection pattern of Area1 shows regular copper reflections while Area2 presents disordered copper reflections (Fig. 4(g)). The former is the pattern of the Cu-rich chalcocite phase and the latter is the pattern of the Cu-deficient djurleite phase.⁴² The two areas are chosen from one single-crystal nanochannel but present different phases, supporting copper migration along the direction of the electric field.

To recap, the thermal annealing of CFs triggers Cu₂S phase transition to the super-ionic phase with liquid Cu⁺, which

migrates along the electric field to aggregate at the heated locations to generate the cation sources. Here, the diffusion coefficient of the fluid-like Cu⁺ in the HC phase is $2 \times 10^{-7} \text{ cm}^2 \text{ s}^{-1}$, as compared with $10^{-8} \text{ cm}^2 \text{ s}^{-1}$ in the LC phase and $10^{-9} \text{ cm}^2 \text{ s}^{-1}$ in the djurleite phase, owing to disordered copper atom distribution and a large number of copper vacancies.⁴³ Fast copper migration under the electric field results in a rapid accumulation of Cu⁺ in the localized cation sources.

Switching failure mechanisms

To reveal the switching failure mechanism of CBTS selectors, the holding state at V_{hold} is monitored to find out the CF morphology of the devices under a large driving current or after massive cycling. Fig. 5(a) shows that the box chart of V_{hold} , *i.e.*, the switching-off voltage, moves toward zero bias with increased I_{CC} , indicating that a smaller electric field is required to maintain the CF connection. A more direct observation of this trend is in the IV curves under different I_{CC} in Fig. S15 (ESI[†]). This V_{hold} change also appears in the Ag/TaO_x/TaO_y/TaO_x/Ag devices and Cu/SiO₂ devices, where the V_{hold} is nearly 0 V at I_{CC} over 100 μA .^{11,44} Our selectors require 0.15 V to prevent diffusion even at 500 μA , which proves to be highly diffusive. Next, the conductance of the disconnecting state at V_{hold} during cycling is recorded in Fig. 5(b), compared with the off-state conductance. Significant leakage with a conductance

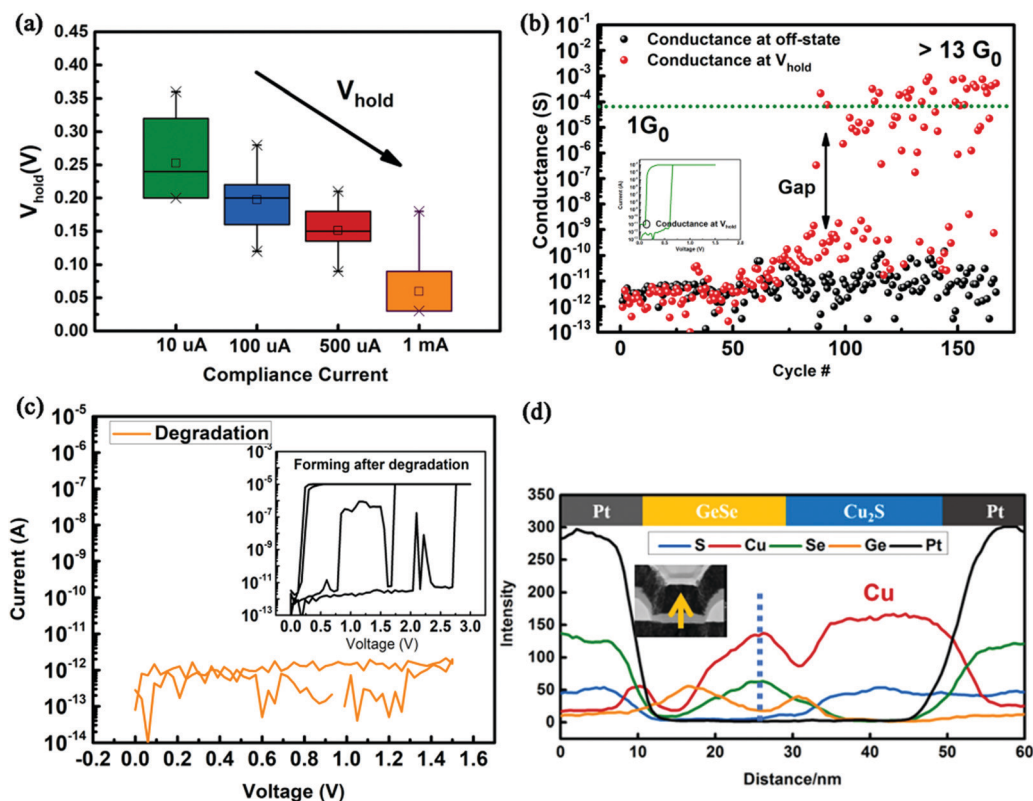


Fig. 5 (a) The switching-off voltage V_{hold} moves toward zero bias along with increased I_{CC} , indicating smaller electric field to maintain the CF connection. (b) The significantly increased conductance after 100th cycles shows that CFs grow thicker after massive cycling. (c) The device failed by being stuck at the HRS and could be recovered by applying a large electric field. (d) EDS line scan on the cross-section of the *via*-hole showing copper aggregation in the middle of GeSe, overlapping with the Se peak.

of $>1 G_0$ (single-atomic-contact conductance) appears at V_{hold} after about the 100th cycle, corresponding to full CF connection,⁴⁵ which can be removed by withdrawing the electric field, as shown in Fig. 5(b). The increased conductance at V_{hold} suggests that CFs get thicker and thus harder to break along with cycling. The maximum conductance is larger than $13 G_0$, which indicates that the thinnest connection of CFs before rupturing is equally thick as 13 atomic channels bound together.¹⁷ But still, CFs in the Pt/Cu₂S/GeSe/Pt selector diffuse back to HRS after the electric field is removed, as indicated by the black balls in Fig. 5(b).

The device finally stuck at HRS after massive cycling, as shown in Fig. 5(c), triggered by copper depletion in the cation sources. The failed devices could be recovered by applying a large electric field (inset in Fig. 5(c)), which is attributed to field-activated copper migration to supply the cation sources. The device failure caused by the exhaustion of the copper reservoirs instead of CF overgrowth and large CF conductance before disconnecting supports the large amount and tiny size of the CFs in the Pt/Cu₂S/GeSe/Pt selector. Next, the atomic rearrangement of the massively cycled devices is investigated by EDS line-scan on the device cross-section, which shows highly concentrated copper in the middle of the GeSe layer (Fig. 5(d)). The peak for the atomic content of copper overlaps with Se peak, suggesting that Se^{2-} combines with Cu^+ to accelerate CF rupture. As a comparison, the line-scan of the non-*via* area in Fig. S16 (ESI[†]) shows slightly and gradually reduced Cu diffusion in GeSe, which was caused by the deposition.

The schematic of the Pt/Cu₂S/GeSe/Pt devices conducting the current is described in Fig. 6. In the range of $0 < V < V_{\text{th}}$, the cation sources inject Cu^+ into GeSe, leading to preferential CFs growth (Fig. 6(a)). When $V > V_{\text{th}}$, these CFs connect TE and BE to conduct the current in parallel, as depicted in Fig. 6(b). The distribution of CFs is dense, enabling multiple CFs to deliver the current at a J_{ON} of 10 MA cm^{-2} even in nanodevices. After V drops below V_{hold} , the CFs are rapidly disrupted, driven by factors described in Fig. 6(c). First, the gradient distribution of the Cu atoms facilitates the diffusion. Second, Se^{2-} in GeSe tends to seize Cu^+ from the CFs. Third, the Cu₂S layer retracts copper back from the contact of the CFs with Cu₂S. More

importantly, the size of the CFs is tiny at the beginning owing to local cation injection from the Cu-rich sources.

Experimental methods

Device fabrication

The Pt/Cu₂S/GeSe/Pt devices were fabricated in 250 nm diameter *via*-hole structure in this work. First, Ti/Pt (10/100 nm) BE was consecutively deposited on the SiO₂/Si substrate through sputter coating. This was followed by 100 nm SiO₂ isolation layer growth *via* thermal plasma enhanced chemical vapor deposition (PECVD). Next, electron beam lithography (EBL) was used to pattern the 250 nm *via*-hole and the BE pad. The subsequent III-V Inductively Coupled Plasma (ICP) etching method revealed the patterns. After that, the TE pattern was introduced by photolithography. 15 nm GeSe and 30 nm Cu₂S films were deposited through pulsed laser deposition (PLD) and sputtering, respectively, followed by 100 nm Pt TE sputtering. The last step is the lift-off. All of the functional material depositions were carried out under room temperature and without post processing.

Device characterizations

DC sweep was implemented using an Agilent B1500A semiconductor Analyzer. In AC pulse measurements, time domain voltage pulse generation and fast current sensing were performed by an Agilent B1531A. During the on/off speed detection, a 45 k Ω resistor was connected in series with the selector to limit the maximum on-state current. The TEM cross-sectional images and EDS composition mapping were acquired by a Field Emission Gun/TEM (FEI Titan themis G2) under 200 kV voltage. The *in situ* XRD pattern was obtained through a Bruker D8 ADVANCE at a heating rate of $5^\circ \text{C min}^{-1}$, and 0.02° per step in a 2θ range from 30° to 50° at a scanning rate of 0.3° s per step.

Thermal simulation

The related information is described in the supplementary note ESI.[†]

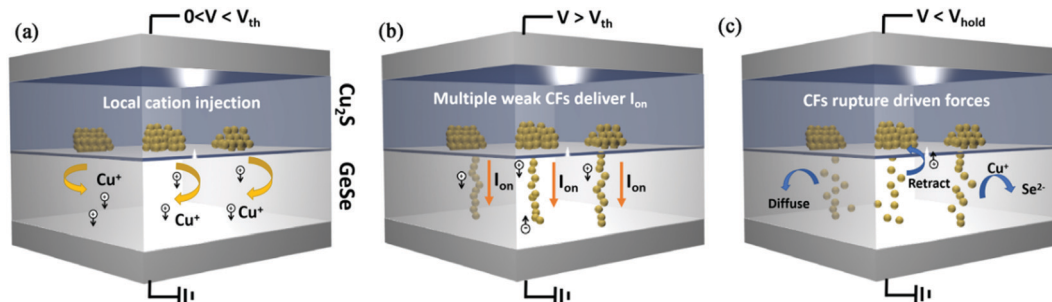


Fig. 6 Schematic of multiple CFs formed by local cation injection after introducing the super-ionic Cu₂S layer. (a) Local cation injection from the Cu-rich cation sources modulates the size and number of CFs. (b) Multiple tiny CFs conduct the current in parallel. (c) CFs rupture driven by Cu concentration gradient in GeSe, Cu₂S retracting effect, and Se^{2-} combination with Cu^+ .

Conclusion

In summary, $10 \text{ MA cm}^{-2} J_{\text{ON}}$ was realized in $\text{Cu}_2\text{S}/\text{GeSe}$ -based selectors by densely localized Cu-rich cation sources to increase the quantity and confine the size of the CFs. The superionic Cu_2S phase with liquid Cu^+ induced by the CF thermal effect encourages field-assisted Cu^+ migration to create local Cu-rich cation sources. Faster cation injection from these Cu-rich cation sources leads to controllable CF growth. Except for the increased quantity of the CFs, the CF size is limited by the size of the sources, thus preventing the overgrowth. As a result, the J_{ON} of CBTS selectors is improved more than ten times while 10^{10} selectivity is realized at the same time, which is applicable for large-scale PCM integration.

Author contributions

Qi Lin and Hao Tong conceived the idea. Qi Lin performed the experiment. Qi Lin, Jinlong Feng, Junhui Yuan, and Long Liu contributed to the formal analysis. Qi Lin, Ming Xu, Jason K. Eshraghian, and Xingsheng Wang contributed to the paper writing. Hao Tong and Ming Xu were in charge and advised on all parts of the project. Xiangshui Miao formulated overarching research goals and aims, also the acquisition of the financial support for the project leading to this publication. All authors discussed and reviewed the manuscript.

Conflicts of interest

There are no conflicts to declare.

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